Online Short Term Training Program

On

Digital system Design with HDL (DSDHDL)

July 13 - Aug 4, 2024

Organized

by

Department of Electronics

&

Communication Engineering

National Institute of Technology Calicut Kerala, India - 673601

About NIT Calicut

National Institute of Technology Calicut (NITC) is fully centrally funded by MHRD and is governed by the NIT Act 2007. Institute has ten departments, three schools and nine research centers. It offers ten UG, and thirty PG programs along with the Ph.D program in various fields of Science, Technology and Engineering. Faculties in the various Departments have active collaborations with universities and elite institutions within and outside India for research and have active consultancy for industries. For details visit the website: www.nitc.ac.in

About the Department

The B.Tech in Electronics & Communication Engineering started in 1980 in the Department of Electrical Engineering. The rapid development in Electronics & Communications initiated the inception of a separate Department of Electronics & Communication Engineering in 1997. The department offers M. Tech programmes, in Electronic Design Technology, Microelectronics & VLSI, Signal Processing and Telecommunication and PhD in related field. The Department is a recognized QIP Centre of the AICTE for both M. Tech and PhD programs. The Department is also actively engaged in R&D activities. For details see our website: www.ece.nitc.ac.in

About the STTP:

The field of Digital System Design is always driven by its applications and advances in VLSI technologies. Hence, challenges are always imposed by them on implementations of Digital systems. Such implementations must satisfy the enforced speed, area and power constraints of real-time Digital Signal Processing applications. The goal of this STTP is to provide critical concepts in the understanding of the state-of-the-art digital system design using Verilog HDL and techniques used to design custom or semi-custom VLSI circuits for various applications. It will cover the concepts from fundamentals to advanced level, giving thrust to implementation of Digital Systems.

Key Highlights

- This STTP focuses on concepts related to Efficient the Digital Circuit Design using HDL.
- Various Design style using HDL will be discussed.
- Sessions will be held on weekends.
- Online Lab Session

Resource Person

All the Resources person will be from the Department of Electronics and Communication Engineering, NIT Calicut.

Registration Detail:

Registration is restricted to **30 participants** only on a first-come, first-served basis.

To register for this STTP, follow the steps

1. Fill an online form by **25th June 2024.**

   https://forms.gle/x9vH43G5i83vwou97

2. Confirmation of the Registration by **28 June 2024.**

3. Payment for STTP by **2nd July 2024.**

Payment Details will be sent to participants along with confirmation email.

Fee for the Participant: INR 2000

E-Certificates will be provided to registered participants upon completion of course.

Who Can Apply?

UG / PG students/ Research Scholars who have already completed or going to complete basic course on Digital Circuits and Systems.

- **NIT Calicut students are not allowed to register for this STTP.**
- **For the online lab participant should have stable high speed internet connection and Xilinx Vivado software or any available open source software for HDL Design and Simulation.**

Faculty Coordinator

Dr. Ashutosh Mishra, Assistant Professor
Department of ECE, NIT Calicut.

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Student Coordinator

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For all the queries please write an email or contact to student coordinator.

Topics to be Covered

This program will cover the following topics:

- Introduction to VLSI Design Flow
- Basics of CMOS Design
- Fundamental of Digital Circuits.
- Combinational Circuit Design.
- Sequential Circuit Design.
- Verilog Hardware Description Language.
- Digital Circuit Implementation in FPGA
- Some Advance Architecture
- Online Hands on Lab Session (6 Hours)

Schedule:

Date	Time	Topic
13th July 2024 (Saturday)	2:00 PM to 5:00 PM	Introduction VLSI Design Flow, Fundamental of VLSI Design
14th July 2024 (Sunday)	2:00 PM to 5:00 PM	Introduction to Verilog HDL, Coding style for synthesis
20th July 2024 (Saturday)	2:00 PM to 5:00 PM	Verilog HDL Continue
21st July 2024 (Sunday)	2:00 PM to 5:00 PM	Introduction to Xilinx Vivado Tool for HDL
27th July 2024 (Saturday)	2:00 PM to 5:00 PM	Combinational Logic Circuit Design Using Verilog HDL
28th July 2024 (Sunday)	2:00 PM to 5:00 PM	Sequential Logic Circuit Design Using Verilog HDL
03rd Aug. 2024 (Saturday)	2:00 PM to 5:00 PM	Some Advance Circuit
04th Aug. 2024 (Sunday)	2:00 PM to 5:00 PM	Lab Session

Expected Outcome

At the end of the STTP, the participants will be able:

• To acquire the insights on digital system design and its realization using FPGA

• To understand the challenges in implementing applications of digital system and their solutions.