M.Tech.

IN

MICROELECTRONICS AND VLSI DESIGN

CURRICULUM AND SYLLABI

(Applicable from 2023 admission onwards)

Department of Electronics and Communication Engineering
NATIONAL INSTITUTE OF TECHNOLOGY CALICUT
Kozhikode - 673601, KERALA, INDIA

The Programme Educational Objectives (PEOs) of M. Tech. in Microelectronics and VLSI Design

PEO1	Graduates apply their theoretical foundation and research skills in Semiconductor devices, VLSI Circuits and Systems and expertise in modern CAD and EDA tools to identify, analyze and solve engineering problems pertaining to Microelectronics and VLSI Design
PEO2	Graduates apply their subject knowledge, communication skills and leadership qualities to build their chosen career in the area of Microelectronics and VLSI Design and allied fields.
PEO3	Graduates exhibit ethical attitude and sensitivity to social, environmental and economic issues in their professional activities.
PEO4	Graduates possess a high level of motivation to continue in their chosen field of career and to acquire greater technical knowledge and develop higher skills as technology advances.

Programme Outcomes (POs) & Programme Specific Outcomes (PSOs) of M.Tech. in Microelectronics and VLSI Design

PO1	An ability to independently carry out research /investigation and development work to solve practical problems.
PO2	An ability to write and present a substantial technical report/document.
PO3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the programme. The mastery should be at a level higher than the requirements in the appropriate bachelor programme.
PSO 1	Competence to take-up challenges in the area of Microelectronics and VLSI Design by possessing strong theoretical foundation and research skills in the state of the art technology.
PSO 2	Ability to engage in continuous learning in the area of Microelectronics & VLSI Design so as to face challenges of the rapidly changing global scenario and come up with innovative ideas for improvement.

CURRICULUM

The minimum number of credits to be earned by a student for the award of the degree is 75. The total credits must not exceed 77.

COURSE CATEGORIES AND CREDIT REQUIREMENTS:

The structure of M.Tech. programme shall have the following Course Categories:

Sl. No.	Course Category	Minimum Credits
1.	Programme Core (PC)	23
2.	Programme Electives (PE)	15
3.	Institute Elective (IE)	2
4.	Projects	35

The effort to be put in by the student is indicated in the tables below as follows:
L: Lecture (One unit is of 50 minute duration)
T: Tutorial (One unit is of 50 minute duration)
P: Practical (One unit is of one hour duration)
O: Outside the class effort / self-study (One unit is of one hour duration)

PROGRAMME STRUCTURE

Semester I

Sl. No.	Course Code	Course Title	L	T	P	O	Credits	Category
1.	EC6101E	Design of Digital Systems	3	0	2	7	4	PC
2.	EC6201E	Digital Integrated Circuit Design	3	0	2	7	4	PC
3.	EC6202E	Analog Integrated Circuit Design	3	0	2	7	4	PC
4.	EC6203E	Advanced Semiconductor Device Modeling	3	0	0	6	3	PC
5.		Elective 1	3	0	0	6	3	PE
6.		Institute Elective					2	IE
		Total					**20**	**--**

Semester II

Sl. No.	Course Code	Course Title	L	T	P	O	Credits	Category
1.	EC6204E	MOS Device Modeling and Fabrication	3	0	2	7	4	PC
2.	EC6205E	VLSI Design Automation	3	0	2	7	4	PC
3.		Elective 2	3	0	0	6	3	PE
4.		Elective 3	3	0	0	6	3	PE
5.		Elective 4	3	0	0	6	3	PE
6.		Elective 5	3	0	0	6	3	PE
7.	EC6296E	Project Phase I	0	0	0	6	2	PC
		Total					**22**	**--**

Semester III

Sl. No.	Course Code	Course Title	L	T	P	O	Credits	Category
1.	EC7297E	Project Phase II	0	0	0	9	3	PC
2.	EC7298E	Project Phase III	0	0	0	45	15	PC
		Total					**18**	--

Semester IV

Sl. No.	Course Code	Course Title	L	T	P	O	Credits	Category
1.	EC7299E	Project Phase IV	0	0	0	45	15	PC
		Total					**15**	--

List of Electives

Institute Elective Basket (Students need to credit Minimum 2 credits from this basket):

Sl. No.	Course Code	Course Title	L	T	P	O	Credits
1	IE6001E	Entrepreneurship Development	2	0	0	4	2
2	ZZ6001E	Research Methodology	2	0	0	4	2
3	MS6174E	Technical Communication and Writing	2	1	0	3	2

Elective Basket 1 (Students need to credit Minimum 3 credits from this basket):

Sl. No.	Course Code	Course Title	L	T	P	O	Credits
1	EC6221E	VLSI Technology	3	0	0	6	3
2	EC6222E	MEMS Structures and Applications	3	0	0	6	3
3	EC6223E	Power Semiconductor Devices and Technology	3	0	0	6	3
4	EC6224E	Compound Semiconductor Devices and Applications	3	0	0	6	3
5	EC6225E	Fundamentals of Photovoltaic Devices	3	0	0	6	3
6	EC6226E	Compact Modelling of Semiconductor Devices	3	0	0	6	3
7	EC6227E	THz Electronics	3	0	0	6	3

Elective Basket 2 (Students need to credit Minimum 3 credits from this basket):

Sl. No.	Course Code	Course Title	L	T	P	O	Credits
1	EC6241E	Analog System Design	3	0	0	6	3
2	EC6242E	CMOS RF IC Design	3	0	0	6	3
3	EC6243E	VLSI Data Converters	3	0	0	6	3
4	EC6244E	Phase-Locked Loops	2	0	2	5	3
5	EC6245E	CMOS Image Sensors	2	0	2	5	3
6	EC6246E	Architectural Design of Digital Integrated Circuits	3	0	0	6	3
7	EC6247E	Digital VLSI Testing	3	0	0	6	3
8	EC6248E	Verification of VLSI Systems	2	0	2	5	3
9	EC6249E	VLSI Digital Signal Processing	3	0	0	6	3
10	EC6250E	Bluespec System Verilog	3	0	0	6	3
11	EC6251E	Low Power VLSI	2	0	2	5	3

Students can credit a maximum of two elective courses, each having minimum 3 credits, from courses offered in any M. Tech. specialization by the Institute, with the consent of the Programme Coordinator and the Course Faculty.

Syllabus for M. Tech in Microelectronics and VLSI Design

EC6101E DESIGN OF DIGITAL SYSTEMS

Pre-requisites: NIL

L	T	P	O	C
3	0	2	7	4

Total Sessions: 39L+26P

Course Outcomes:

CO1: Interpret the constructs of Hardware Description Language.

CO2: Design digital circuits and model them at different levels of abstraction.

CO3: Develop synthesizable RTL code targeting ASIC/FPGA.

CO4: Identify the problems with synchronous designs and address them.

Lecture Sessions:

Introduction to digital design methodology using HDL - Design flow - Modeling abstraction levels, gate level model, RTL model, behavioral model - Simulation and synthesis - Modeling for ASIC/FPGA - Language concepts - Data types and operators - Structural, data flow and behavioral models - Hierarchical structure - Combinational and sequential circuit description - Continuous and procedural assignments - Blocking and non-blocking assignments - Tasks and functions - Interfaces - Delay modeling - Parameterized reusable design - System tasks - Compiler directives - Testbenches.

Datapath and controllers - Complex state machine design - Modeling FSMs - State encoding - Modeling memory - Basic pipelining concepts - Pipeline modeling - Clock domain crossing - Modeling of arithmetic functions - Impediments to synchronous design: clock skew, gating the clock, asynchronous inputs, synchronizer failure and metastability - Synchronizer design - Synchronizing high speed data transfers - Timing analysis.

Introduction to synthesis - Logic synthesis - RTL synthesis - High-level synthesis, Synthesis of combinational logic, priority structures, sequential logic with latches and flip-flops - Unintentional latches - Synthesis of state machines - Registers and counters - Clocks - Loops - Code optimizations - Design examples - Programmable LSI techniques - PLA/PAL/PLDs - CPLD and FPGAs - Xilinx/Altera series FPGAs - Programmable System on Chip - Zynq SoC design overview.

Practical sessions:

Introduction to HDL simulator, design and testbench code, backtrace and debug using waveform viewer – Model combinational/sequential logic circuits using structural, data flow and behavioral models – Model finite state machines in different styles – Synthesis and backend flow for FPGA – Implementation of digital circuits/systems on reconfigurable devices – Debug using ILA – Create custom IP and reuse.

References:

1. Stuart Sutherland, Simon Davidmann, Peter Flake, *SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling*, Second Edition, Springer Science & Business Media, 2006.
2. Michel D. Ciletti, *Advanced digital design with the Verilog HDL*, Second Edition, Pearson, 2010.
3. John F Wakerley, *Digital Design Principles and Practice*, Fifth Edition, Pearson education, 2018
4. J. Bhasker, *Verilog HDL Synthesis: A Practical Primer*, B. S. Publications, 2001.
5. Crockett LH, Elliot RA, Enderwitz MA, Stewart RW, *The Zynq Book: Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable Soc*, Strathclyde Academic Media, 2014.

EC6201E DIGITAL INTEGRATED CIRCUIT DESIGN

Pre-requisites: NIL

L	T	P	O	C
3	0	2	7	4

Total Sessions: 39L+26P

Course Outcomes:

CO1: Appreciate device and system level knowledge required to realize integrated circuits

CO2: Analyze the operation of CMOS logic circuits and develop models to estimate the circuit specifications

CO3: Design and simulate static and dynamic CMOS logic circuits for given functionality, speed, power consumption and area requirements.

CO4: Design and simulate error-free sequential and memory circuits

Lecture Sessions:

Review of MOSFET, threshold voltage, current, body effect, short channel effects, velocity saturation, mobility degradation - CMOS inverter and its operation - Static characteristics, noise margin, effect of process variation, supply scaling - Dynamic characteristics, effective switching resistance and capacitance, delay, effect of input rise time and fall time, driving large capacitances - Static and dynamic power dissipation, energy and power delay product, impact of load capacitance on power consumption

Multiple input static CMOS logic circuits, DC and transient analysis, area, power and noise margin - Logical and electrical effort, parasitic delay, branch effort, high speed circuit design using logical effort - Pass gates and transferring logic levels, delay through pass gates, complementary pass transistor logic and transmission gates – DCVSL - Dynamic logic, speed and power, noise in dynamic logic, Domino logic and its derivatives, C^2MOS, TSPC registers, NORA CMOS

Designing sequential circuits, latches and register design - Timing basics, set up time, hold time – Memory design, SRAM and DRAM cells-Interconnection delay, driving long wires, interconnection noise, electro migration, antenna diode-Power supply noise and decoupling capacitors-I/O circuits and ESD clamp

Practical sessions:

Introduction to SPICE simulator, schematic entry and cell generation, test bench - MOSFET characteristics and parameter extraction – Static and dynamic characteristics of logic circuits, corner analysis, Monte Carlo simulation – Layout generation, design rule check, layout Vs schematic, parasitic extraction, post-layout simulation – Standard cell layout, characterization - Design of memory cells,

References:

1. David Hodges, Horace Jackson, Resve Saleh, *Digital Integrated Circuits in Deep Submicron Technologies*, McGraw Hill, 3rd Edition, 2004.
2. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, *Digital Integrated Circuits- A Design Perspective*, Pearson, 2nd Edition, 2016.
3. Ivan E. Sutherland, Robert F. Sproull, David F. Harris, *Logical Effort: Designing Fast CMOS Circuits*, Morgan Kaufmann, 1999.
4. S.M. Kang, Y. Leblebici, Chul Woo Kim, *CMOS Digital Integrated Circuits Analysis and Design*, 4th Edition, McGraw Hill, 2014.
5. R. Jacob Baker, *CMOS Circuit Design, Layout, and Simulation*, 3rd Edition, Wiley-IEEE Press, 2010

EC6202E ANALOG INTEGRATED CIRCUIT DESIGN

Pre-requisites: NIL

L	T	P	O	C
3	0	2	7	4

Total Sessions: 39L+26P

Course Outcomes:

CO1: Model various components in CMOS process to estimate their performance in circuits.

CO2: Obtain the design of the biasing circuits for CMOS amplifiers.

CO3: Design single stage amplifiers and various stages of an operational amplifier.

CO4: Design operational amplifiers and comparators to meet the given specifications

CO5: Perform the custom design flow of analog circuits using CAD tools for a given set of speculations.

Lecture Sessions:

CMOS Process Circuit Components

MOS transistor: 4 terminal MOS transistor model, threshold voltage, drain current, body bias effect, channel length modulation - Small signal model of the MOS transistor, low frequency MOSFET model, influence of body effect on small and large signal behavior of analog circuits - High frequency MOSFET model, transit frequency

Biasing and Amplification

Current sources and sinks, Current mirrors, matching considerations in current mirrors, concept of current steering - Self biasing circuits, Constant Gm biasing - Start-up circuits - Bandgap referenced biasing, voltage references
Single stage amplifiers – Telescopic cascode amplifier, folded cascade amplifier, differential amplifier- Frequency response of the amplifiers - Noise: Resistor noise, kT/C across a capacitor; MOS transistor noise, MOS transistor thermal and flicker noise - Noise in single-stage amplifiers, noise in current mirrors and differential Pairs, input referred noise - MOS transistor mismatch, effect of transistor mismatch in amplifiers and current mirrors

Operational Amplifiers

Operational amplifiers - Negative feedback and stability, loop gain and unity loop gain frequency, feedback compensation-Op amp offset, swing limits, slew rate - Design of single stage and multistage operational amplifiers - Noise in operational amplifier, effect of transistor mismatches in the performance of operational amplifiers
Fully differential op amps, analysis of fully differential circuits using common-mode and differential half circuits - Common mode feedback, CMFB circuits, common mode feedback loop stability, fully differential two-stage op amp

Comparators

CMOS comparator, Comparator parameters: sensitivity, offset, speed, power dissipation, power supply rejection, input capacitance, kickback noise, metastability, input CM range - Comparator design issues, offset cancellation, correlated double sampling, differential comparators, latches, pre amplifier stages

Practical Sessions

Introduction to SPICE simulator - MOSFET characteristics and small signal parameter extraction – Biasing and amplifier circuits, transient analysis, frequency response, noise analysis, corner analysis, Monte Carlo simulation – Layout design of analog circuits –Design and simulation of single-stage/two-stage operational amplifiers, characterization and documentation.

References:

1. B.Razavi, *Design of Analog CMOS Integrated Circuit*, 2nd Edition McGraw Hill India, 2017
2. P. Allen & D. Holberg, *CMOS Analog Circuit Design*, 3rd Edition, Oxford University Press, 2013
3. R.J. Baker, *CMOS Circuit Design, Layout and Simulation*, 3nd Edition, Wiley-Blackwell , 2010
4. Gray, Hurst, Lewis and Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th Edition, Wiley India, 2011

EC6203E ADVANCED SEMICONDUCTOR DEVICE MODELING

Pre-requisites: NIL

L	T	P	O	C
3	0	0	6	3

Total Sessions: 39L

Course Outcomes:

CO1: Apply the qualitative understanding of physics of semiconductors to develop quantitative models for semiconductor phenomena relevant to the field of electronics

CO2: Model semiconductor junction and characterize p-n junction diodes

CO3: Model and characterize Metal oxide semiconductor junctions and Metal oxide semiconductor FETs.

Review of semiconductor physics – Quantum foundations - Semiconductor band structure, simplified band structure models, carrier concentration – Non equilibrium – Quasi Fermi levels - Drift and diffusion – Mobility – Generation and recombination

Analysis of p-n junction under equilibrium and bias – Energy band diagram – Diode current equation – Break down of p-n junctions

Metal oxide semiconductor junction – Capacitance - voltage characteristics – Threshold voltage – Effect of work function difference and insulator charges

Metal Oxide Semiconductor Field effect transistors – Current–voltage characteristics – Sub threshold operation- Substrate bias effects – Short channel effects and MOSFET scaling

References:

1. Nandita Das Guptha and Amithava Das Guptha, Semiconductor Devices, Modeling and Technology, PHI India, 2004.
2. C. C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, Pearson 2010
3. S.M. Sze and Kwok K. Ng, *Physics of Semiconductor Devices*, Wiley, 2007
4. M. K. Achuthan and K. N. Bhatt, *Fundamentals of Semiconductor Devices*, McGraw-Hill, 2009.
5. B.L. Anderson and R. L. Anderson, *Fundamentals of Semiconductor Devices*, McGraw-Hill, 2005
6. Research articles and technical reports in the area of semiconductor device experimentation and modeling

EC6204E MOS DEVICE MODELING AND FABRICATION

Pre-requisites: NIL

L	T	P	O	C
3	0	2	7	4

Total Sessions: 39L+26P

Course Outcomes:

CO1: Review the operation and modeling of the MOS Capacitor and MOSFETs

CO2: Analyze and model small dimension effects in modern MOSFETs

CO3: Review the MOSFET fabrication processes

CO4: Familiarize the use of TCAD tools in semiconductor device and process simulation

Lecture Sessions:

MOS Capacitor – Contact potentials – Insulator charges – Flat band voltage – Potential Balance and charge Balance – Effect of gate body voltage on MOS surface conditions – Small signal capacitance –Body effect

MOSFET – Regions of operation – Complete all region model - Strong inversion, weak inversion and moderate inversion – Effective mobility – Temperature effects

Small channel and thin oxide effects – Carrier velocity saturation – Channel length modulation - Charge sharing – Drain induced barrier lowering - Punch through – Hot carrier effects – Polysilicon depletion – Quantum mechanical effects – Junction leakages - Scaling

Planar MOSFET fabrication process – NMOS, PMOS and CMOS process – Fabrication of non-conventional MOSFET devices

Practical sessions:

Simulation of the MOSFET characteristics using TCAD simulators and validation of experimental characteristics available in literature – C-V characteristics of a MOS Capacitor- I-V characteristics of MOSFETs – simulation of short channel effects – mobility effects – process simulation

References:

1. Y. Tsividis and Colin McAndrew**,** *The MOS Transistor***,** 3rd Edition, Oxford University Press, 2013**.**
2. Narain Arora**,** *MOSFET modeling for VLSI simulation: Theory and Practice***,** World Scientific, 2007.
3. Yuan Taur and Tak H Ning, *Fundamentals of Modern VLSI Devices***,** Cambridge University Press, 2013.
4. C. C. Hu, *Modern Semiconductor Devices for Integrated Circuits***,** Pearson, 2010
5. A. B. Bhattacharya, *Compact MOSFET Models for VLSI Design***,** John Wiley, 2009
6. Research articles and technical reports in the area of semiconductor device experimentation, modeling and fabrication

EC6205E VLSI DESIGN AUTOMATION

Pre-requisites: NIL

L	T	P	O	C
3	0	2	7	4

Total Sessions: 39L+26P

Course Outcomes:

CO1: Identify the issues at various stages of VLSI physical design.

CO2: Develop algorithms to solve the complex physical design problems in ICs.

CO3: Analyze and optimize the algorithms that help in the back end design of complex chips.

CO4: Apply physical design techniques and design an IC for specific area, delay and power requirements.

Lecture Sessions:

Introduction to digital IC design - Custom and semicustom flow, combinational logic synthesis - Technology independent and technology dependent optimization - Binary decision diagrams - High level synthesis- Scheduling and allocation – Physical design – Terminology – Basic Unix/Linux commands – Introduction to C shell/Perl scripting.
Partitioning - Constructive and iterative algorithms - Kernighan-Lin algorithm - Fiduccia-Mattheyses algorithm - Multilevel partitioning, clustering

Simulated annealing and evolution – Floor planning - Slicing and non-slicing floor plan - Polish expression - Constraint based, analytical, rectangular dual graph, hierarchical tree methods - Pin assignment – General and channel pin assignment – Placement – Cost function – Simulation, partitioning and performance based placement algorithms.

Routing – Global routing - Maze routing, line search, Steiner tree based algorithms – Detailed routing–Constraint graphs – Channel routing - Left edge algorithm – Dog leg routing – Switch box routing –
Over the cell routing – Clock network design considerations - Clock tree synthesis - Power and ground routing - Static timing analysis and timing closure.

Practical sessions:

Introduction to back end automation tools - perl scripting - ASIC design flow from HDL coding to GDSII layout – Design, synthesis, floorplanning, placement, routing - use of fast, typical, slow standard cell libraries - report analysis - design rule check, layout Vs schematic checks - post clock tree synthesis and pre clock tree synthesis analysis

References:

1. Andrew B. Kahng, Jens Lienig, Igor L. Markov and Jin Hu, *VLSI Physical Design: from graph partitioning to timing closure*, 2nd Edition, Springer Science & Business Media, 2022.
2. Wang, Laung-Terng, Yao-Wen Chang, and Kwang-Ting Tim Cheng, *Electronic design automation: synthesis, verification, and test*, Morgan Kaufmann, 2009.
3. Gerez and Sabih H., *Algorithms for VLSI Design Automation*, John Wiley & Sons, 2006
4. Naveed A. and Sherwani, *Algorithms for VLSI Physical Design Automation*, Springer, 3rd Edition, *1999.*

EC6296E PROJECT PHASE I

Pre-requisites: NIL

L	T	P	O	C
0	0	0	6	2

Course Outcomes:

CO1: Survey the literature on new research areas and compile findings on a particular topic

CO2: Organize and illustrate technical documentation with scientific rigor and adequate literal standards on the chosen topic strictly abiding by professional ethics while reporting results and stating claims

CO3: Develop aptitude for research and independent learning.

CO4**:** Demonstrate communication skills in conveying the collected data through technical reports and oral presentations using modern presentation tools.

The objective of this phase of the project is to impart training to the students in collecting materials on a specific topic in the broad domain of Engineering/Science from books, journals and other sources, compressing and organizing them in a logical sequence, and presenting the matter effectively both orally and in written format. The topic should not be a replica of what is contained in the syllabi of various courses of the M. Tech programme. The topic chosen by the student shall be approved by the project guide(s) and the evaluation committee. Based on the collected information and acquired knowledge, the student is expected to identify unresolved problems in the domain of the selected topic.

EC7297E PROJECT PHASE II

Pre-requisites: NIL

L	T	P	O	C
0	0	0	9	3

Course Outcomes:

CO1: Develop aptitude for research and independent learning

CO2: Demonstrate the ability to select unresolved problems in the domain of the selected project topic and explore suitable solutions

CO3: Gain the expertise to use new tools and techniques for the design and development.

CO4**:** Demonstrate communication skills in conveying the collected data through technical reports and oral presentations using modern presentation tools.

The work carried out in EC7297E Project Phase II is a continuation of EC6296E Project Phase I and to be continued in EC7298E and/or EC7299E. In these project phases, students get an opportunity to apply and extend knowledge acquired in the first and second semesters of their M. Tech. programme. The work will be carried out individually. The objective of the Project Phase II is to identify unresolved problems in the domain of the selected topic (if not done at the end of the second semester) and explore possible solutions. The proposed solution(s) shall be compared with the ones which are available in the literature or in practice using suitable methods along with a feasibility study. The work can be analytical, simulation, hardware design or a combination of these in the emerging areas of Microelectronics and VLSI Design under the supervision of a faculty from the ECE Department.

At the end of Project Phase II, students are expected to have a clear idea of the work to be done, and have learnt the analytical / software / hardware tools. Presenting preliminary designs and results are highly desirable. The students are also expected to submit an interim technical report including the project work carried out in this phase and the work plan for the forthcoming semester(s).

EC7298E PROJECT PHASE III

Pre-requisites: NIL

L	T	P	O	C
0	0	0	45	15

Course Outcomes:

CO1: Develop aptitude for research and independent learning

CO2: Acquire the knowledge and awareness to carry out cost-effective and environment friendly designs.

CO3: Gain the expertise to use new tools and techniques for the design and development.

CO4**:** Develop the ability to write good technical report, to make oral presentation of the work, and to publish the work in reputed conferences/journals.

The work carried out in EC7298E Project Phase III is a continuation of EC7297E Project Phase II and shall be continued in EC7299E or it can be an internship work carried out in an industry. In both cases, the work will be carried out individually. The objective of the Project Phase III is to design/develop the solution proposed in the Project Phase II using one or more of the following approaches: (i) Analytical models (ii) Computer simulations (iii) Hardware implementation. The project work of a student during the third semester is evaluated by a committee in two phases.

If a student plans for an internship in the fourth semester or exploring a different project topic in the fourth semester after doing the Project Phase III in the institute, the student should complete the work planned in the beginning of the third semester, attaining all the objectives and shall prepare a project report of the complete work starting from Project phase I to Project Phase III. If a student plans to continue the same work in the Project phase IV, a detailed project report should be submitted at the end of the Project Phase IV. In case of an internship, the work will be decided jointly by the guides of the student both in the institute and the internship organization. A detailed internship report shall be prepared and submitted by the student.

EC7299E PROJECT PHASE IV

Pre-requisites: NIL

L	T	P	O	C
0	0	0	45	15

Course Outcomes:

CO1: Develop aptitude for research and independent learning

CO2: Acquire the knowledge and awareness to carry out cost-effective and environment friendly designs.

CO3: Gain the expertise to use new tools and techniques for the design and development.

CO4**:** Develop the ability to write good technical report, to make oral presentation of the work, and to publish the work in reputed conferences/journals.

The work carried out in EC7299E Project Phase IV is a continuation of EC7298E Project Phase III or it can be an internship work carried out in an industry. The students are expected to communicate their innovative ideas and results to reputed conferences and/or journals. The work carried out by the students in Project Phase IV will be evaluated in two phases.

IE6001E ENTREPRENEURSHIP DEVELOPMENT

Pre-requisites: NIL

L	T	P	O	C
2	0	0	4	2

Total Lecture Sessions: 26

Course Outcomes:

CO1: Describe the various strategies and techniques used in business planning and scaling ventures.

CO2: Apply critical thinking and analytical skills to assess the feasibility and viability of business ideas.

CO3: Evaluate and select appropriate business models, financial strategies, marketing approaches, and operational plans for startup ventures.

CO4: Assess the performance and effectiveness of entrepreneurial strategies and actions through the use of relevant metrics and indicators.

Entrepreneurial Mindset and Opportunity Identification

Introduction to Entrepreneurship Development - Evolution of entrepreneurship, Entrepreneurial mindset, Economic development, Opportunity Recognition and Evaluation - Market gaps - Market potential, Feasibility analysis - Innovation and Creativity in Entrepreneurship - Innovation and entrepreneurship, Creativity techniques, Intellectual property management.

Business Planning and Execution

Business Model Development and Validation - Effective business models, Value proposition testing, Lean startup methodologies - Financial Management and Funding Strategies - Marketing and Sales Strategies - Market analysis, Marketing strategies, Sales techniques - Operations and Resource Management - Operational planning and management, Supply chain and logistics, Stream wise Case studies.

Growth and Scaling Strategies

Growth Strategies and Expansion - Sustainable growth strategies, Market expansion, Franchising and partnerships - Managing Entrepreneurial Risks and Challenges - Risk identification and mitigation, Crisis management, Ethical considerations - Leadership and Team Development - Stream wise Case studies

References:

1. Kaplan, J. M., Warren, A. C., & Murthy V. (Indian Adoption) (2022). *Patterns of entrepreneurship management*. John Wiley & Sons.
2. Kuratko, D. F. (2016). *Entrepreneurship: Theory, process, and practice*. Cengage learning.
3. Barringer, B. R. (2015). *Entrepreneurship: Successfully launching new ventures*. Pearson Education India
4. Rajiv Shah, Zhijie Gao, Harini Mittal, *Innovation, Entrepreneurship, and the Economy in the US, China, and India*, 2014, Academic Press
5. Dr. K. Sundar, *Entrepreneurship Development*, 2nd Ed 2022 Vijaya Nichkol Imprints, Chennai
6. E. Gordon,Dr. K. *Natarajan,Entrepreneurship Development*, 6th Ed, 2017, Himalya Publishers,Delhi
7. Debasish Biswas, Chanchal Dey,*Entrepreneurship Development in India*, 2021, Taylor & Francis

ZZ6001E RESEARCH METHODOLOGY

Pre-requisites: NIL

L	T	P	O	C
2	0	0	4	2

Total Lecture sessions: 26

Course Outcomes:

CO1: Explain the basic concepts and types of research

CO2: Develop research design and techniques of data analysis

CO3: Develop critical thinking skills and enhanced writing skills

CO4: Apply qualitative and quantitative methods for data analysis and presentation

CO5: Implement healthy research practice, research ethics, and responsible scientific conduct

Exploring Research Inquisitiveness
Philosophy of Scientific Research, Role of Research Guide, Planning the Research Project, Research Process, Research Problem Identification and Formulation, Variables, Framework development, Research Design, Types of Research, Sampling, Measurement, Validity and Reliability, Survey, Designing Experiments, Research Proposal, Research Communication, Research Publication, Structuring a research paper, structuring thesis/ dissertation,

Research Plan and Path
Developing a Research Plan: Reviewing the literature- Referencing – Information sources – Information retrieval – Role of libraries in information retrieval – Tools for identifying literatures – Reading and understanding a research article – Critical thinking and logical reasoning; Framing the research hypotheses, Converting research Question into a Model; Data collection- Types of data-Dataset creation- Primary and Secondary data- Scales of measurement- Sources and collection of data- Processing and analysis of data-Understanding Data-statistical analysis, displaying of data-Data visualization-Data interpretation; Research design- Qualitative and Quantitative Research- Designing of experiments- Validation of experiments- Inferential statistics and result interpretation

Scientific Conduct and Ethical Practice
Plagiarism– Ethics of Research- Scientific Misconduct- Forms of Scientific Misconduct. Plagiarism, Unscientific practices in thesis work-Conduct in the workplace and interaction with peers – Intellectual property: IPR and patent registration, copyrights; Current trends – Usage and ethics of AI tools in scientific research.

References:

1. Leedy, P D, "*Practical Research: Planning and Design",* USA: Pearson, Twelfth ed., 2018.
2. Krishnaswamy, K. N., Sivakumar, A. I., and Mathirajan, M., "*Management Research Methodology"*, Pearson Education, 2006.
3. Tony Greenfield and Sue Greener., *Research Methods for Postgraduates*, USA: John Wiley & Sons Ltd., Third ed., 2016.
4. John W. Creswell and J. David Creswell, "*Research Design: Qualitative, Quantitative, and Mixed Methods Approaches*", USA: Sage Publications, Sixth ed., 2022

MS6174E TECHNICAL COMMUNICATION AND WRITING

Pre-requisites: NIL

L	T	P	O	C
2	1	0	3	2

Total Lecture Sessions: 26

Course Outcomes:

CO1: Apply effective communication strategies for different professional and industry needs.

CO2: Collaborate on various writing projects for academic and technical purposes.

CO3: Combine attributes of critical thinking for improving technical documentation.

CO4: Adapt technical writing styles to different platforms.

Technical Communication

Process(es) and Types of Speaking and Writing for Professional Purposes - Technical Writing: Introduction, Definition, Scope and Characteristics - Audience Analysis - Conciseness and Coherences - Critical Thinking - Accuracy and Reliability - Ethical Consideration in Writing - Presentation Skills - Professional Grooming - Poster Presentations

Grammar, Punctuation and Stylistics

Constituent Structure of Sentences - Functional Roles of Elements in a Sentence - Thematic Structures and Interpretations - Clarity - Verb Tense and Mood - Active and Passive Structures - Reporting Verbs and Reported Tense - Formatting of Technical Documents - Incorporating Visuals Elements - Proofreading

Technical Documentation

Types of Technical Documents: Reports, Proposals, Cover Letters - Manuals and Instructions - Online Documentation - Product Documentation - Collaborative Writing: Tools and Software - Version Control Document Management - Self Editing, Peer Review and Feedback Processes

References:

1. Foley, M., & Hall, D. (2018). *Longman advanced learner's grammar, a self-study reference & practice book with answers*. Pearson Education Limited.
2. Gerson, S. J., & Gerson, S. M. (2009). *Technical writing: Process and product*. Pearson.
3. Kirkwood, H. M. A., & M., M. C. M. I. (2013). *Hallidays introduction to functional grammar* (4th ed.). Hodder Education.
4. Markel, M. (2012). *Technical Communication* (10th ed.). Palgrave Macmillan.
5. Tuhovsky, I. (2019). *Communication skills training: A practical guide to improving your social intelligence, presentation, Persuasion and public speaking skills.* Rupa Publications India.
6. Williams, R. (2014). *The Non-designer's Design Boo*k. Peachpit Press.

EC6221E VLSI TECHNOLOGY

Pre-requisites: NIL

L	T	P	O	C
3	0	0	6	3

Total Lecture Sessions: 39

Course Outcomes:

CO1: Analyze the basics of crystal growth, wafer preparation and wafer cleaning

CO2: Model the oxidation growth and diffusion mechanism in semiconductors

CO3: Analyze the lithography, etching and deposition process

CO4: Verify processes and device characteristics via simulations

Semiconductor Crystal Growth and Wafer Engineering

Historical perspective, semiconductor manufacturing, processing overview, Crystal growth- Electronic grade silicon, Czochralski growth, Bridgman growth, Float zone growth, Si wafer characterization and properties of Silicon wafers, clean rooms, gettering and wafer cleaning.

Fabrication Processes-I

Deposition- Thin films deposition, evaporation, E-beam and resistive heating evaporation, Sputtering, PLD and chemical vapor deposition. Epitaxy- molecular beam epitaxy, vapor phase epitaxy, liquid phase epitaxy, ALD, evaluation of epitaxial layers. silicon oxidation- Thermal oxidation process, kinetics of growth, Deal-Grove model, properties of Silicon dioxide, oxide quality, high κ and low κ dielectrics –Lithography - photo-reactive materials, pattern generation and mask making, pattern transfer, photolithography, electron beam, Ion beam and X-ray lithography- Etching- Wet and dry etching, reactive ion etching, plasma and ion beam techniques

Fabrication Processes-II

Diffusion- Diffusion process, modeling of diffusion, diffusion in a concentration gradient, impurity behaviour, diffusion systems, problems in diffusion, evaluation of diffused layers - Ion Implantation- Types Ion Implantation, modeling of Ion implantation, penetration range, Ion implantation systems, process considerations, implantation damage and rapid thermal annealing

Process Integration

Device Isolation - Junction and oxide isolation, LOCOS, shallow trench isolation, contacts and Metallization- Schottky contacts, ohmic contacts, planarization techniques - Integration of processes for bipolar - N well, P-well and Twin tub CMOS, BiCMOS fabrication processes -Defining system rules for IC layout - Packaging - Die-bonding, wire-bonding, flip-chip technology - Future trends and challenges- Challenges for integration, system on chip

References:

1. S.K. Ghandhi, *VLSI Fabrication principles*, John Wiley Inc., 2008
2. S.M. Sze, *VLSI Technology*, 4th Edition, McGraw Hill Co. Inc., 1999
3. James Plummer, M. Deal and P.Griffin, *Silicon VLSI Technology*, Prentice Hall Electronics, 2010
4. R.C. Jaeger, *Introduction to microelectronic fabrication*, Prentice Hall, Second Edition, 2013

EC6222E MEMS STRUCTURES AND APPLICATIONS

Pre-requisites: NIL

L	T	P	O	C
3	0	0	6	3

Total Lecture Sessions: 39

Course Outcomes:

CO1: Gain knowledge of basic approaches for various MEMS sensors and actuators design.

CO2: Capability to critically analyze microsystems technology for technical feasibility as well as practicality.

CO3: Develop efficient MEMS design for improving device performance in terms of speed, sensitivity Selectivity and accuracy

CO4: Design and analysis of efficient MEMS sensors and actuators

MEMS Materials and Micromachining Technology
Overview of Nano and Microelectromechanical Systems and Applications-Review of Electrical and Mechanical concepts in MEMS- Stress and strain analysis, Mechanics including elasticity, beam bending theory, cantilevers, Membranes, and plates. Materials for MEMS and NEMS-Silicon, silicon compounds, polymers, and metals. MEMS fabrication technologies- Micromachining- Bulk Micromachining, Surface Micromachining, Silicon Etching, LIGA Process - Assembly of 3D MEMS – Foundry process.

Sensors and Actuators I
Piezoresistive sensors – Piezoresistive sensor materials, Stress analysis of mechanical elements, Design of cantilevers and Membranes Piezoresistive sensor, Applications to Inertia, Pressure, Tactile and Flow sensors. Electrostatic Sensing and Actuation- Design parallel plate Capacitive and Comb drive actuators, Pull-in Effect, Applications to Inertia, Pressure, Tactile and Flow sensors, Micro-motor, MEMS RF switches, Thermal actuators- Fundamentals of thermal transfer, Thermal bimorph principle, Thermal couples, resistors and their applications

Sensors and Actuators II
Piezoelectric sensors and actuators – piezoelectric effects – piezoelectric materials – Applications to Inertia, Acoustic, Tactile and Flow sensors, Microphone, Micro speaker, Nanogenerator, RF resonator, Acoustic wave sensors, SAW filter- Magnetic Actuation- Fabrication of Micro Magnetic Components, Case Studies of MEMS Magnetic Actuators. Bio-MEMS- Chemoresistors, Chemocapacitors, Chemotransistors, Electronic nose (E-nose)

Calibration and Packaging Techniques
Basic Fluid Mechanics Concepts, Micro Fluidics Applications. Case Studies- Gyros. MEMS device Calibration and packaging techniques- Device Design Considerations, Types of packaging, Hermetic or Nonhermetic Packaging, Wafer Dicing, Wafer Bonding, Reliability Market Uncertainties, Investment, and Competition. MEMS software: COMSOL & Intellisuite.

References:

1. Chang Liu, *Foundations of MEMS*, Prentice Hall, 2006.
2. Tai Ran Hsu, *MEMS and Microsystems Design and Manufacture*, Tata Mcraw Hill, 2002.
3. Albert Folch, *Introduction to BioMEMS*, CRC, 2012.
4. Edward Lyshevski, *MEMS and NEMS: Systems, Devices, and Structures*, CRC Press, 2002.

EC6223E POWER SEMICONDUCTOR DEVICES AND TECHNOLOGY

Pre-requisites: NIL

L	T	P	O	C
3	0	0	6	3

Total Lecture Sessions: 39

Course Outcomes:

CO1: Analyze the physics of breakdown mechanism in power semiconductor devices.
CO2: Interpret the existing models for Silicon power MOSFET and IGBT.
CO3: Interpret the operation of Silicon Carbide power MOSFET.

Silicon power diodes - Avalanche breakdown voltage of silicon planar p-n junctions, breakdown voltage improvement techniques – Floating field rings – Field plates - MESA structures. High injection level effects in pn junctions- power BJT

Silicon Power MOSFETs, I-V characteristics, on resistance, minimum size chip design for specific drain breakdown voltage, switching characteristics, safe operating area, Insulated Gate Bipolar Transistor (IGBT) – Structure, operation principle, I-V characteristics and turn off transients, latch up and its prevention.

Silicon Carbide power devices – Advantages of Silicon Carbide over Silicon from high power point of view– SiC diodes – Avalanche breakdown voltage – SiC power MOSFETs – Different SiC power MOSFET architectures – on state I-V characteristics – Break down voltage improvement - SiC IGBT- GaN power devices

References:

1. Baliga, B. Jayant, *Power Semiconductor Devices*, PWS Publishing Co., Boston, 1996.
2. B. J. Baliga., *Silicon Carbide Power Devices*, World Scientific, 2006.
3. B. J. Baliga, *Gallium Nitride and Silicon Carbide Power Devices*, World Scientific, 2017.
4. HongyuYu, TianliDuan, *Gallium Nitride Power Devices*, Pan Stanford, 2017
5. Research articles and technical reports in the area of Power semiconductor device experimentation, modeling and Fabrication.

EC6224E COMPOUND SEMICONDUCTOR DEVICES AND APPLICATIONS

Pre-requisites: NIL

L	T	P	O	C
3	0	0	6	3

Total Lecture Sessions: 39

Course Outcomes:

CO1: Interpret important parameters governing the high speed performance of devices and circuits

CO2: Model the properties of hetero junctions from the energy band diagram point of view

CO3: Model the physics and operation and modeling of MESFETs

CO4: Interpret the operation and performance parameters of HEMT, HBTs and Optoelectronics Devices

Basic Properties of Compound Semiconductors
Important parameters governing the high speed performance of devices and circuits: Transit time of charge carriers, junction capacitances, ON-resistances and their dependence on the device geometry and size, carrier mobility, doping concentration and temperature - Materials properties: Merits of III –V binary and ternary compound semiconductors (GaAs, InP, InGaAs, AlGaAs, SiC, GaN etc.), different SiC structures, silicon-germanium alloys and silicon carbide for high speed devices, as compared to silicon based devices - Band diagrams, homo and hetero junctions.

Metal Semiconductor related parameters and devices
Metal semiconductor contacts and Metal Insulator Semiconductor and MOS devices: Native oxides of Compound semiconductors for MOS devices and the interface state density related issues. Metal semiconductor Field Effect Transistors (MESFETs): Basic features, Pinch off voltage and threshold voltage.

HEMT, HBTs and Optoelectronics Devices
High Electron Mobility Transistors (HEMT): The generic Modulation Doped FET (MODFET) structure for high electron mobility realization, Principle of operation and the unique features of HEMT. Hetero junction Bipolar transistors (HBTs): Principle of operation and the benefits of hetero junction BJT for high speed applications. Optoelectronic Devices: Basic working principles and performance parameters of LED, Photodetectors and Solar Cell.

References:

1. B. J. Baliga, *Gallium Nitride and Silicon Carbide Power Devices*, World Scientific, 2017.
2. Sandip Tiwari, *Compound Semiconductor Device Physics*, Academic Press, 1992.
3. Robert F. Pierret, *Semiconductor Device Fundamentals*, Addison-Wesley 1996.
4. S. M. Sze, *High-Speed Semiconductor Devices*, Wiley, 1990.
5. Avishay Katz, *Indium Phosphide and Related materials: Processing, Technology and Devices*, Artech House, 1992.

EC6225E FUNDAMENTALS OF PHOTOVOLTAIC DEVICES

Pre-requisites: NIL

L	T	P	O	C
3	0	0	6	3

Total Lecture Sessions: 39

Course Outcomes:

CO1: Describe the requirements for the effective design and processing of photovoltaic devices.

CO2: Demonstrate various Photovoltaic devices fabrication and characterization techniques

CO3: Design the Photovoltaic Devices and Modules

Basics of Solar Cell

Solar resource, air mass, need of solar PV, prospects of PV technology, light absorption, charge excitation, charge drift/diffusion, charge separation, charge collection - PN junction diodes: Dark IV, illuminated IV - device performance parameters - Series/ Shunt resistance - Factors affecting the performance parameters - Losses and conversion efficiency limit - Generations of solar cell.

Fabrication and Characterization of Solar Cells

Fabrication: Chemical Vapor Deposition (CVD), Physical Vapor Deposition (PVD: Sputtering, Electron Beam Evaporation, Pulsed Laser Deposition, Atomic Layer Deposition), electrodeposition, spin coating - Characterization: Solar simulator, quantum efficiency measurement, XPS/UPS, FESEM, energy dispersive X-Ray spectroscopy, photo-luminescence

Cutting Edge Themes, PV modules and PV Device Modelling

Light manipulation in PV devices: Plasmonic integration, surface texturing, spectrum splitting techniques - Advance PV technologies: Multijunction, quantum well, concentrator, hot electron solar cell - PV modules: Series and parallel connection, parameters, fabrication and lifetime testing - PV device modeling: Hands-on with an open source tool.

References:

1. Smets Arno et al., *Solar Energy Fundamentals, Technology, and Systems*, UIT Cambridge. 2013
2. Martin A. Green, *Solar Cells: Operating Principles, Technology and System Applications*, Prentice Hall, 1986.
3. Jenny Nelson, *The Physics of Solar cells*, World Scientific, 2003.
4. D. K. Schroder, *Semiconductor Material and Device Characterization*, Wiley Interscience, 2006
5. Konrad Mertens, *Photovoltaics Fundamentals, Technology, and Practice*, Wiley, 2018,
6. J. Poortmans and V. Arkhipov, *Thin Film Solar Cells: Fabrication, Characterization and Applications*, Willey, 2006.

EC6226E COMPACT MODELING OF SEMICONDUCTOR DEVICES

Pre-requisites: Semiconductor device physics

L	T	P	O	C
3	0	0	6	3

Total Lecture Sessions: 39

Course Outcomes:

CO1: Implement compact models for circuit simulation in Verilog-A

CO2: Compare charge and surface potential based modeling approaches

CO3: Develop compact models for advanced semiconductor devices

Introduction to SPICE simulator; Basic principles of physical device simulation (TCAD) and compact models, application of compact model, existing industry-standard compact models, implementation of compact models using hardware descriptive languages (Verilog-A), Verilog-A details and coding practices, mathematics for compact modeling

Compact modeling of two and three terminal devices: Integrated resistor and Inductor and MOSCAP - MOSFET modeling approaches – Threshold voltage (BSIM3 and BSIM4), charge based (EKV, BSIM6), surface-potential based (PSP; BSIMCMG, ASM-HEMT); MOSFET Modeling – Core model, terminal current, terminal charges, terminal capacitances, short-channel effects, self-heating effect

Advanced concepts: MOSFET model for RF application - Noise models, NQS effects, parasitic elements, modeling of process variability, concept of binning - Benchmark test of MOSFET compact models; Advanced devices compact model – Multigate FETs, FDSOI, Nanosheets, Tunnel FETs, GaN HEMT, NC-FETs, Magnetic Devices; Case Study on development of Industry Standard Compact Models – BSIM4, BSIM6, PSP, HiSIM, ASM-HEMT, MVSG - Parameter extraction procedure - Device Characterization and its importance in compact model development.

References:

1. G. Gildenblat, *Compact Modeling: Principles, Techniques and Applications*, Springer, 2010
2. W. Liu, *MOSFET Models for SPICE Simulation: Including BSIM3v3 and BSIM4*, Wiley, 2001.
3. Y. S. Chauhan et.al., *FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG standard*, Academic Press, 2015.
4. S. K. Saha *Compact Models for Integrated Circuit Design: Conventional Transistors and Beyond*, CRC Press, 2016.
5. Y. Tsividis, *Operation and Modeling of the MOS Transistor*, McGraw Hill, 1999
6. N. Arora, *MOSFET Modeling for VLSI Simulation: Theory and Practice*, World Scientific, 2007
7. C. C. Enz, E. A. Vittoz, *Charge Based MOS Transistor Modeling: The EKV Model for Low power and RF IC Design*, John Wiley & Sons, Ltd., 2006.
8. G. Massobrio, P. Antognetti, *Semiconductor Device Modeling with SPICE*, McGraw Hill Book Co., 1988.

EC6227E THz ELECTRONICS

Pre-requisites: NIL

L	T	P	O	C
3	0	0	6	3

Total Lecture Sessions: 39

Course Outcomes:

CO1: Understand the specifications of THz electronics system and applications of THz Electronics

CO2: Design on-chip THz electronics using integrated active and passive components

CO3: Distinguish between different THz sources and detection methods.

Introduction to THz science and technologies; THz Gap; Terahertz interaction in molecular- and atomic-scale - Terahertz systems specifications: Active vs passive, broadband vs narrowband, time domain vs frequency domain, coherent vs incoherent, far-field vs near-field, power vs field - THz Applications: THz communication, THz Imaging, THz spectroscopy.

CMOS passives at THz - Metal stacks, capacitors, inductors, transmission lines, on-chip antennas; Transistors at THz - Transistor power gain, f_T and f_{max}, gate resistance, technology comparison; THz in CMOS/BiCMOS above f_{max}; Calibration/de-embedding methodologies – On-chip and off-chip, Thru-reflect-line, short-open, load-thru, line-reflect-match and line-reflect-reflect-match - De-embedding Techniques.

THz Sources: Traditional THz sources- vacuum device sources, diode sources - Gunn dodes, IMPATT diodes, resonant tunneling diodes (RTDs) - Transistor based THz sources - Harmonic generators, oscillators; optical THz sources - THz photomixing.
THz Detectors: Detector figures of merits - Thermal detectors – Bolometers, Golay cells, pyroelectric; diode detectors - Schottky Barrier Diodes (SBDs), SIS Mixers, superconducting hot electron Bolometers (HEBs) - Transistor and transistor circuit detectors; Direct detection, heterodyne detection.

References:

1. G. Carpintero, L.E. Garcia Munoz, S. Preu, H. Hartnagel, and A.V. Räisänen, *Semiconductor THz Technology: From Components to Systems*, John Wiley & Sons, 2015
2. H. Wang and K. Sengupta, *RF and mm-Wave Power Generation in Silicon*, Academic Press, 2015
3. J.-S. Rieh, *Introduction to Terahertz Electronics*, Cham: Springer Nature, 2021
4. J.-H. Son, *Terahertz biomedical science and technology*, CRC Press, 2014.
5. X.-C. Zhang and J. Xu *Introduction to THz Wave Photonics*, Springer, 2010
6. J. H. Choi, *High-Speed Devices and Circuits with THz Applications*, CRC Press, 2017

EC6241E ANALOG SYSTEM DESIGN

Pre-requisites: Design of two stage op amp in CMOS process

L	T	P	O	C
3	0	0	6	3

Total Lecture Sessions: 39

Course Outcomes:

CO1: Design of high-performance op-amps

CO2: Make use of the knowledge of continuous-time filters to realize discrete switched-capacitor filters

CO3: Design of continuous-time filters

CO4: Understand the analog design issues in the nanometer regime

High performance op amps
Frequency compensation in feedback amplifiers, review of Miller compensation, feed forward topologies - Gain boosting in amplifiers - Low power and low noise, low offset op-amps - High slew rate, class AB biasing - Analog circuit layout- Op amp design using a SPICE tool
.

Discrete-time and continuous-time filters
Resistor emulation using a MOSFET and capacitor, charge injection, clock feed-through, switched capacitor integrators, non-overlapping clock - Switched capacitor gain circuits - First order and second order filters, switch sharing, low-Q and high-Q biquad filters, op-amps for switched capacitor circuits - Gm-C filters, CMOS transconductors, active RC and MOSFET-C filters, frequency and Q-factor tuning - Design and simulation of filters

Analog circuits at nanometer regime
Nanometer design issues, transistor design, design for given drain current and transconductance, choice of length, op amp design examples, small signal and large signal behaviour, op amp scaling - Design and simulation of two stage op amp/folded cascode op amp

References:

1. J. Huijsing, *Operational amplifiers Theory and design*, 3rd Edition, Springer, 2017.
2. P. Allen and D. Holberg, *CMOS Analog Circuit Design*, 3rd Edition, Oxford University Press, 2013
3. R. Gregorian and G. C. Temes, *Analog MOS integrated circuits for signal processing*, Wiley India Pvt Limited, 1986.
4. T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, 2nd Edition, John Wiley & Sons, 2012.
5. B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd Edition, McGraw Hill Education, 2015.
6. Research articles and technical reports in the area of analog circuits

EC6242D CMOS RF IC DESIGN

Pre-requisites: NIL

L	T	P	O	C
3	0	0	6	3

Total Lecture Sessions: 39

Course Outcomes:

CO1: Demonstrate an understanding of the language, basic operation of basic RF modules.

CO2: Relate to the inventory of RF device models.

CO3: Design of RF modules to meet the given specifications.

CO4: Apply the understanding to the design of wireless systems and other allied fields appreciating the trade-offs between noise, linearity, spectral cost etc.

Basics of RF Circuit Design

Linearity and distortion: Third-order intercept point, second-order intercept point, 1-dB compression point, broadband measures of linearity - Modeling of active & passive components at high frequencies - Noise: Available noise power, noise figure- Impedance matching: broadband matching, power matching & noise matching - High frequency amplifiers: Bandwidth estimation using open-circuit & short-circuit time constants - using zeros to enhance bandwidth - shunt-series amplifiers, tuned amplifiers & cascaded amplifiers

RF Amplifiers

RF power amplifiers: Design of class A, AB, B, C, D, E, F, G & H amplifiers - Low-noise amplifier (LNA), CS, CG & cascode amplifiers, Feedback amplifiers - Noise & linearity of amplifiers - Amplifiers using differential configurations - Low voltage topologies for LNA, DC bias networks for LNA, design of broadband LNA, Case studies of RF power amplifiers and LNAs

Mixers and Oscillators

Mixers: Mixing operation, Mixing with nonlinearity, Mixer noise and linearity, Mixer with local oscillator switching, popular mixer configurations like the Moore mixer, mixer with simultaneous noise and power match, mixer employing current reuse for low power applications

Oscillators: Negative resistance-based LC resonator, Colpitts oscillator, Differential topologies, Phase noise in oscillators - Tunable oscillators -Phase-locked loops (PLL), PLL components, in-band and out-of-band phase noise, Frequency synthesizers

References:

1. John W M Rogers & Calvin Plett, *Radio Frequency Integrated Circuit Design*, 2nd Edition, Artech House, 2010
2. Richard Chi-Hsi Li, *RF Circuit Design*, John Wiley & Sons, 2009
3. Hooman Darabi, *Radio Frequency Integrated Circuits & Systems*, Cambridge University Press, 2015
4. Behzad Razavi, *RF Microelectronics*, 2nd Edition, Prentice Hall, 2012
5. Thomas H Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd Edition, Cambridge University Press, 2004.

EC6243E VLSI DATA CONVERTERS

Pre-requisites: Design of two stage op amp and comparators in CMOS process

L	T	P	O	C
3	0	0	6	3

Total Lecture Sessions: 39

Course Outcomes:

CO1: Understand the static and dynamic specifications of data converters

CO2: Design of DACs to meet the given specifications

CO3: Analyze the performance of analog-to-digital converters and choose the configuration suitable for an application

CO4: Design and simulate the building blocks of data converters

Sampling and data converter specifications
Sampling, nonidealities in sampling, noise and distortion in sampling, - sample and hold circuits, timing issues in sample and hold circuit - design and simulation of bootstrapping switches, charge injection and noise - introduction to switched capacitor circuits, switched capacitor sample and hold circuits - static specifications of data converters, accuracy, nonlinearity, offset - dynamic specifications, SNR, SFDR, ENOB, dynamic range
.

Nyquist-rate data converters
Digital-to-analog converter configurations, current steering DAC, segmentation, static and dynamic errors, accuracy, calibration, dynamic element matching, decoders and matrix DAC architecture design - Flash ADC, impacts of latch meta-stability, kick-back noise and offset, sub ranging and pipeline converter architectures, 1.5 bit/stage and error correction, folding and interleaving architectures - SAR ADC - Design and simulation of comparators/current steering DAC

Oversampling data converters
Oversampling and quantization noise spectrum, linearity with oversampling, first-order noise shaping, delta-sigma modulator with noise shaping, switched capacitor implementation, linearized analysis, stability of delta-sigma modulators - decimation filters with accumulate and dump, averaging without decimation, aliasing, interpolation filters for DAC - second order noise shaping, linearity, idle tones and dithering – multi-stage noise shaping architectures, error-feedback structures – behavioural/SPICE level simulation study of oversampling ADCs

References:

1. R. J. Baker, *CMOS Mixed-Signal Circuit Design*, Wiley India Edition, 2009.
2. R. Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, 2nd Edition, Springer, 2007.
3. S. Pavan, R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*, 2nd Edition, John Wiley & Sons, 2017.
4. M. J. M. Pelgrom, *Analog-to-Digital Conversion*, Springer, 2010.
5. T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, 2nd Edition, John Wiley & Sons, 2014.
6. Research articles and technical reports in the area of VLSI data converters

EC6244E PHASE-LOCKED LOOPS

Pre-requisites: Design of differential amplifiers and digital logic gates in CMOS process

L	T	P	O	C
2	0	2	5	3

Total Sessions: 26L + 26P

Course Outcomes:

CO1: Design and simulate the building blocks of PLLs

CO2: Model and analyse PLL systems

CO3: Assess the impact of various noise sources and nonidealities in a PLL system using suitable approaches

CO4: Integrate building blocks of PLL to realize its applications

Lecture Sessions:

Basic PLL topology, Dynamics of simple PLL, XOR phase detector, drawbacks of simple PLL - Phase frequency detector and charge pump, Charge pump PLL, PFD/CP nonidealities, Up and down skew, Channel length modulation, Random mismatches, Clock feedthrough and charge injection, improved charge pumps - Loop filter, loop dynamics and stability analysis, higher order loops - Ring and LC oscillators, Tuning in oscillators, Voltage controlled oscillators

.

Noise in various building blocks of PLL, Noise in time and frequency domains, Jitter and phase noise in PLLs, Phase noise and power trade-off - Integer-N and fractional-N frequency synthesizers, prescalers and dividers, spur reduction techniques - All digital PLLs, All-digital phase detectors, All-digital loop filters, digitally controlled oscillators

Practical sessions:

Transfer characteristics of phase detectors – Charge pumps with improved accuracy – Loop filters -Design of oscillators, introducing tenability to achieve voltage controlled oscillations, phase noise simulations - Integration of the building blocks to realize a PLL, simulation and characterization, jitter and lock time – Modeling of all digital PLLs, synthesis, characterization

References:

1. B. Razavi, *Design of CMOS phased-lock loops: From circuit level to architectural level*, Cambridge university press, 2020.
2. R. Best, *Phase-Locked Loops: Design, Simulation, and Applications*, McGraw Hill, 2003.
3. F. Gardner, *Phase lock Techniques*, John Wiley & Sons, 2005.
4. W. Egan, *Phase-Lock Basics*, John Wiley & Sons, 2008.
5. Research articles and technical reports in the area of phase-locked loops

EC6245E CMOS IMAGE SENSORS

Pre-requisites: NIL

L	T	P	O	C
2	0	2	5	3

Total Sessions: 26L+26P

Course Outcomes:

CO1: Compare the performance of various pixels and choose suitable architecture for an application

CO2: Distinguish various noise sources in image sensors and apply suitable noise reduction techniques for the readout under consideration

CO3: Design building blocks of an image sensor readout

CO4: Develop architecture/application -dependent design optimizations in the readout of an image sensor

Lecture Sessions:

Pixel circuits
Review of MOS capacitor and MOSFET, charge transfer and charge coupled systems, limitation of CCDs - Photodiodes in a standard CMOS technology, photo-generated charges, photo current – Pixel circuits: Passive pixel and its limitation, 3-T active pixels, fill factor, full well capacity, sensitivity, signal dependent non-idealities, reset, temporal and photon shot noise, dark current, signal-to-noise ratio, dynamic range, fixed pattern noise, double sampling techniques, correlated double sampling, pinned-photodiode, 4-T active pixel

Readout circuits
Readout architectures, pixel, column and chip level readouts, column amplifier and sensitivity, adaptive gain column amplifiers, column-level ADCs, slope, cyclic and SAR ADCs, column-shared architectures, low noise readouts, high dynamic range imagers – Applications of image sensors: Event-driven pixels, time-of-flight pixels - Characterization of an image sensor

Practical sessions:
Photodiode model, active pixel circuits, temporal and fixed-pattern noise minimization, double sampling technique, – Column readout: Multiple sampling, amplifiers, analog-to-digital converters – High dynamic range pixel circuits and readouts - Layout design techniques for pixel, column and chip level blocks - Application specific pixel circuits

References:

1. J. Nakamura, *Image Sensors and Signal Processing for Digital Still Cameras*, CRC Press, 2005
2. A. Theuwissen, *Solid-State Imaging with Charge-Coupled Devices*, Kluwer academic publishers, 1995.
3. K. D. Stefanov, *CMOS Image Sensors*, IOP Publishing, 2022
4. J. R. Janesick, *Photon Transfer DN*, SPIE press, 2007.
5. T. Kuroda, *Essential Principles of Image Sensors*, CRC Press, 2015.
6. Research articles and technical reports in the area of CMOS image sensors

EC6246E ARCHITECTURAL DESIGN OF DIGITAL INTEGRATED CIRCUITS

Pre-requisites: NIL

L	T	P	O	C
3	0	0	6	3

Total Lecture Sessions: 39

Course Outcomes:

CO1: Compare the various methodologies of architectural design of digitals ICs

CO2: Optimize an algorithm and map it into an efficient architecture

CO3: Design of low-area and low-power architectures for data paths

Introduction to VLSI Design Flow; Digital design using static CMOS, transmission gates, etc- Area, power and delay considerations in digital design, optimizations in digital design - Number representation and formats.

Mapping an Algorithm into Architecture: Concept of hierarchical system design, algorithms and their architectures (minimum/maximum, GCD, running average, summation of N numbers, etc.) - Control structure design, critical path and worst case timing analysis
Data path optimization and worst case timing analysis: Efficient adder architectures, sign and unsigned multiplier architectures, Braun's multiplier, Baugh-Wolley multiplier, divider and square root design- Application specific combinational and sequential circuit design.

Advance architecture design: CORDIC, extension of CORDIC to cover the full range of angles - FFT Architecture; Parallel and pipeline processing, array architecture - Systolic architecture design: Introduction, systolic array design methodology, applications to signal processing problems.

References:

1. Frank Vahid, *Digital Design with RTL Design, VHDL, and Verilog***,** Wiley, 2011.
2. Behrooz Parhami**,** *Computer Arithmetic: Algorithms and Hardware Designs***,** Oxford University Press, 2010.
3. Sung-Mo Kang, Yusuf Leblebici, Chul Woo Kim, *CMOS Digital Integrated Circuits Analysis & Design***,** 4th Edition, McGraw-Hill, 2014.
4. Research articles and technical reports in the area of architectural design of digital integrated circuits

EC6247E DIGITAL VLSI TESTING

Pre-requisites: NIL

L	T	P	O	C
3	0	0	6	3

Total Lecture Sessions: 39

Course Outcomes:

CO1: Develop test patterns required to detect faults in a circuit

CO2: Determine the testability of a circuit

CO3: Design methods/techniques to improve the testability of digital circuits.

CO4: Design Logic BIST circuits based on LFSRs

Faults and Test pattern generation

Introduction to VLSI Testing process - need and challenges, Faults in Digital Circuits - Controllability, and Observability, Fault models - stuck-at faults, Bridging faults, intermittent faults, Fault equivalence, Fault collapsing and Fault dominance, Logic Simulation and Fault simulation - Serial, Parallel, Deductive and Concurrent Fault Simulation, Combinational and Sequential SCOAP testability Measures

Combinational Circuit Test Pattern Generation - Fault table, Boolean Difference, Path Sensitization Methods, D-Algorithm, PODEM, FAN algorithm,

ATPG for Single-Clock Synchronous Circuits – Nine Valued Logic and Time-Frame Expansion Methods,

Delay fault testing, IDDQ Testing, Test optimization and fault coverage

Design for testability

Design for testability (DFT) - Testability analysis, Scan design-scan design rules, tests for scan circuits, Scan architectures, DFT based Sequential Circuit Testing - Adhoc design for testability - Test Point Insertion, Scan chains, Partial Scan Design, Random Access Scan, Boundary scan standard – Boundary scan cell, TAP controller, modes of operation, EXTEST, INTEST, BYPASS instructions, Fault models for PLAs, Bridging and delay faults and their tests.

Built in Self-Test

Built in Self-Test (BIST) - Design rules, Test pattern generation for BIST - Exhaustive testing, Pseudo-random testing, Pseudo-exhaustive testing, LFSR for pattern generation and Output response analysis, SISR, MISR, Test compression: Test stimulus compression, Test response compaction, Architectures for test compression,

Memory BIST – Type of memory faults, Fault modeling, Fault detection by MARCH tests, Issues in test and verification of complex chips, embedded cores and SOCs, System testing and test for SOCs

References:

1. Bushnell Michael and Vishwani Agrawal, *Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits*, Vol. 17, Springer Science & Business Media, 2004.
2. Wang Laung-Terng, Cheng-Wen Wu, and Xiaoqing Wen, *VLSI test principles and architectures: design for testability*, Academic Press, 2006.
3. Abramovici Miron, M. A. Breuer and A. D. Friedman, *Digital Systems testing and testable design*, Computer Science Press, 1990.
4. Roth Jr, Charles H. and Lizy K. John, *Digital systems design using VHDL*, Nelson Education, 2016.

EC6248E VERIFICATION OF VLSI SYSTEMS

Pre-requisites: A hardware description language

L	T	P	O	C
2	0	2	5	3

Total Sessions: 26L+26P

Course Outcomes:

CO1: Understand verification approaches and formulate a verification plan.

CO2: Develop HVL based deterministic and random self-checking test benches.

CO3: Design and develop reusable layered test benches.

CO4: Apply techniques to assess the verification progress using coverage concepts.

Lecture Sessions:

Introduction to functional verification - HDL and HVL languages - Functional verification approaches, requirements specification and the verification plan – levels of verification – self checking test benches, deterministic and random test bench, layered test bench - code coverage, functional coverage, coverage driven random based approach - Introduction to System Verilog - data types, arrays, structures – procedural statements and routines – design hierarchy – interfaces.

High level modeling, data abstraction, OOPS – interprocess communication – randomization, constrained random verification - Functional coverage, Cover group, Cover point bins, cross coverage – System Verilog assertions - System on chip verification – system level and block level verification - OVM/UVM basics.

Practical sessions:

Self-checking testbenches - Deterministic and random testbenches – Constructs of HVL, data types, arrays, structures, procedural statements, routines, interfaces – Interprocess communication – Constrained randomization – Code coverage - Functional coverage, covergroup, coverpoint bins – Automated regression runs – Layered testbenches.

References:

1. Sutherland, Stuart, Davidmann, Simon, Flake, Peter, *System Verilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling*", Second Edition, Springer Science & Business Media, 2006.
2. Chris Spear, Greg Tumbush, *System Verilog for Verification: A Guide to Learning the Test bench Language Features*, 3rd Edition, Springer Science & Business Media, 2012.
3. Bergeron, J., *Writing Test benches using System Verilog*, Springer, USA, 2006.
4. Rashinkar P, Paterson P, Singh L., *System-on-a-chip verification: methodology and techniques*, Springer Science & Business Media; 2007

EC6249E VLSI DIGITAL SIGNAL PROCESSING

Pre-requisites: NIL

L	T	P	O	C
3	0	0	6	3

Total Lecture Sessions: 39

Course Outcomes:

CO1: Identify different representations of DSP Algorithms.

CO2: Distinguish between different parameters related to hardware implementation of DSP systems.

CO3: Apply different techniques for changes in speed, area and power consumption of the systems.

CO4: Design a DSP system with the given constraints and implement using Hardware Description Language (HDL).

CO5: Appraise different hardware architectures of digital filters.

Introduction to DSP Systems - Representation of DSP Algorithms - Critical path - Loop bound - Iteration bound - Algorithms for computation of iteration bound - Pipelining and parallel processing: Pipelining and parallel processing for low power, pipelining and parallel processing of FIR Filters - Retiming: Definitions and properties, solving system of inequalities, retiming technique - Unfolding: Definition, algorithm for performing unfolding, applications of unfolding - Folding: Definition, folding transformations, register minimization techniques

Systolic architecture design: Introduction, systolic array design methodology, FIR systolic arrays, selection of scheduling vector, matrix-matrix multiplication and 2D systolic array design - CORDIC based implementations: Architecture, implementation of FIR filter and FFT algorithm - Bit-Level arithmetic architectures: Parallel multipliers, bit-serial multipliers, bit-Serial FIR filter design and implementation - Distributed arithmetic and its variants - Canonic sign-digit arithmetic - Subexpression elimination - Multiple constant multiplication

Fast convolution: Cook-Toom algorithm, Winograd algorithm - Low-power design: Theoretical background, scaling versus power consumption, power analysis, power reduction techniques, power estimation approaches - Scaling and roundoff noise: State variable description of digital filters, roundoff noise in digital filters - Architectures for Digital Filters - Implementation of a digital system using Field Programmable Gate Array (FPGA) - Case study on hardware implementation of a DSP system

References:

1. Keshab K. Parhi, *VLSI Signal Processing Systems, Design and Implementation*, John Wiley & Sons, 2008.
2. Lars Wanhammar, *DSP Integrated Circuits*, Academic Press, 1999.
3. Roger Woods, John McAllister, Ying Yi, and Gaye Lightbody, *FPGA-based implementation of signal processing systems*, John Wiley & Sons, 2008.
4. R.G. Lyons, *Understanding Digital Signal Processing*, Pearson Education, 2004.
5. Bhattacharyya, S.S., Deprettere, E.F., Leupers, R., Takala, J. (Eds.), *Handbook of SignalProcessing Systems*, 2nd Edition, 2013.

EC6250E BLUESPEC SYSTEM VERILOG

Pre-requisites: Verilog

L	T	P	O	C
3	0	0	6	3

Total Lecture Sessions: 39

Course Outcomes:

CO1: Identify different lexical elements of Bluespec System Verilog (BSV).

CO2: Distinguish between different statements and expressions of BSV.

CO3: Design a digital system using BSV.

Introduction to Bluespec System Verilog (BSV) - Lexical Elements: Whitespace and comments, Identifiers and Keywords, Integer literals, Real literals, String literals, Don't care values, Compiler directives - Structure of BSV design: Scopes, name clashes and qualified identifiers, Prelude package - Types: Polymorphism, Provisos, deriving clauses - Modules, interfaces and instances: Module definition and instantiation, Interface declaration and instantiation, module and interface instantiation, rules in modulate definition, synthesizing modules.

Static and dynamic semantics - User defined types: Type synonyms, enumerations, structs and tagged unions - Variable declarations and statements: Variable and array declaration and initialization, variable assignment, implicit declaration and initialization, register reads and writes, begin-end statements, conditional statements, loop statements, function definitions - Expressions: Don't care expressions, conditional expressions, unary and binary operators, bit concatenation and selection, begin-end expressions, actions and action blocks, actionvalue blocks, function calls, method calls, static type assertions, struct and union expressions, interface expressions, rule expressions.

Pattern matching: Case statements with pattern matching, case expressions with pattern matching, pattern matching in if statements and other contexts, pattern matching assignment statements - Finite state machines - Important primitives - Guiding the compuler with attributes - Type classes and provisos - Embedding verilog and C in a BSV design.

References:

1. Rishiyur S. Nikhil and Kathy R. Czeck, BSV by Example: The next-generation language for Electronic System Design, Bluespec,2010.
2. R. Nikhil, "Bluespec System Verilog: efficient, correct RTL from high level specifications," *Proceedings. Second ACM and IEEE International Conference on Formal Methods and Models for Co-Design, 2004. MEMOCODE '04.*, San Diego, CA, USA, 2004, pp. 69-70,
3. Arvind and R. Nikhil, "Hands-on Introduction to Bluespec System Verilog (BSV)," *2008 6th ACM/IEEE International Conference on Formal Methods and Models for Co-Design*, Anaheim, CA, USA, 2008, pp. 205-206.

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EC6251E LOW POWER VLSI

Pre-requisites: CMOS digital circuits

L	T	P	O	C
2	0	2	5	3

Total Lecture Sessions: 39

Course Outcomes:

CO1: Minimize the power consumption in CMOS circuits using voltage and frequency scaling

CO2: Apply different levels of optimizations to reduce switched capacitances

CO3: Identify different methods to reduce leakage power consumption

CO4: Realize different low power techniques in the logic circuits

Lecture Sessions:

Review of power dissipation in CMOS Circuits: Sources of power dissipation, static, dynamic and leakage power dissipation - Dynamic power reduction - Supply voltage scaling approaches: Optimal transistor Sizing with voltage scaling, parallelism, pipelining, optimal supply voltage, using multiple supply voltage, mltiple device threshold, dynamic voltage and frequency scaling - Feature size scaling - Threshold voltage scaling - Transistor sizing for energy minimization

Minimizing Switched Capacitance: Switching activity reduction, algorithmic optimization, architecture optimization, logic optimization, circuit optimization - Different logic style, static and dynamic logic - Clock gating - Reducing glitches through path balancing, input reordering
Leakage Reduction Techniques: Transistor stacks, power gating, multi-threshold CMOS, variable threshold CMOS, dynamic threshold CMOS - Adiabatic circuits -Asynchronous system basics

Practical sessions:

Design and synthesis of logic circuits incorporating different techniques to reduce power - The effect of pipelining and parallel processing on power and speed – Power reduction using Clock gating in the synchronous circuits – Dynamic logic and power consumption – Variation in power, speed and area with Transistor sizing – Multiple threshold circuits

References:

1. Roy Kaushik and Sharat C. Prasad, *Low-power CMOS VLSI Circuit Design*, John Wiley & Sons, 2009.
2. Yeap Gary K, *Practical Low Power Digital VLSI Design*, Springer Science & Business Media, 2012.
3. Bellaouar Abdellatif, Mohamed Elmasry, *Low-Power Digital VLSI design: Circuits and Systems*, Springer Science & Business Media, 2012.
4. Piguet C, *Low-Power CMOS Circuits: Technology, Logic Design and CAD tools*. CRC Press, 2005.
5. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Digital *Integrated Circuits- A Design Perspective*, Pearson, 2nd Edition, 2016.