CURRICULUM AND SYLLABUS OF
M.TECH. DEGREE PROGRAMME IN
MICROELECTRONICS AND VLSI DESIGN

(Applicable from 2010 admission)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY CALICUT

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

National Institute of Technology Calicut

Vision of the Department of Electronics and Communication Engineering:

The Department of Electronics and Communication Engineering is envisioned to be a leading centre of higher learning with academic excellence in the field of electronics and communication engineering.

Mission of the Department in pursuance of its vision:

The mission of the Department of Electronics and Communication Engineering is to impart high quality technical education by offering undergraduate, graduate and research programs in the domain of Electronics and Communication Engineering with thorough foundation in theory along with strong hands-on design and laboratory components, tools and skills necessary for the students o become successful major contributors to society and profession.

PEOs and Programme Outcomes: PG EC 62 :Microelectronics and VLSI Design

Programme Educational Objectives (PEOs):

Sl. No.	Program Educational Objectives
PEO 1	To provide graduates strong theoretical foundation in the area of Microelectronics and VLSI Design and enable them to take up the challenges of the current technology.
PEO 2	To impart research skills with the aid of modern TCAD tools so that graduates can come up with solutions to the challenging problems in the area of Microelectronics and VLSI Design and formulate innovative ideas through independent thinking and Reflective Learning
PEO 3	To impart research skills and encourage continuous learning and improvement in the area of Microelectronics & VLSI Design so that the graduates feel confident enough to face the challenges of the rapidly changing global scenario.
PEO 4	To upkeep the highest values of professionalism and ethical attitude and nurture the ability to relate engineering issues to broader social context.

Programme Outcomes (POs)

The student who completes the Master of Technology in Microelectronics and VLSI Design will be able to

Sl. No.	Program Outcome	Graduate Attribute
PO 1	Acquire in-depth knowledge in the broad area of Microelectronics and VLSI Design and allied disciplines, with an ability to discriminate, evaluate, analyze and synthesize the acquired knowledge.	Scholarship of Knowledge
PO 2	Analyze complex problems in the domain of Microelectronics and VLSI Design critically to make intellectual and creative advances for conducting research in a wider, theoretical, and practical and policy context.	Critical Thinking
PO 3	Solve problems in the area of Microelectronics and VLSI Design imparting lateral thought and originality.	Problem Solving
PO 4	Develop skills to extract information on research problems through literature survey and apply appropriate research methodologies, techniques and tools to design and conduct experiments, analyze and interpret data and demonstrate higher order skills to contribute individually or in groups to the development of scientific or technological knowledge Microelectronics and VLSI Design.	Research Skill
PO 5	Model and simulate problems in the area of Microelectronics & VLSI Design by using modern tools and interpret the data to propose innovative ideas.	Usage of Modern Tools
PO 6	Possess knowledge and understanding of group dynamics, recognize opportunities and contribute positively to collaborative-multidisciplinary scientific research in the area of Microelectronics and VLSI Design.	Collaborative and Multidisciplinary Work
PO 7	Demonstrate knowledge and understanding of engineering and management principles and apply the same to one's own work, as a member and leader in a team, with dues consideration of economical and financial factors in the area of Microelectronics & VLSI Design.	Project Management and Finance

PO 8	To express ideas with clarity and communicate confidently and effectively to the international community through reports adhering to appropriate standards and/or oral presentations using audio and / video supplements.	Communication
PO 9	Recognize the need to engage in life-long learning with a high level of enthusiasm and commitment to improve knowledge in the domain of Microelectronics and VLSI Design.	Life-long Learning
PO 10	Acquire professional and intellectual integrity, professional code of conduct and ethics of research, considering the impact of research outcome on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.	Ethical Practices and Social Responsibility
PO 11	Independently and critically analyze and make corrective measures for continuous improvement, without external feedback.	Independent and Reflective Learning

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Curriculum for M. Tech. in Microelectronics and VLSI Design

Semester 1

S. No.	Code	Name of the Subject	L	T	P/S	C
1.	EC6201	Basics of VLSI	3	0	3	4
2.	EC6202	Semiconductor Device Theory and Modelling	3	0	0	3
3.	EC6203	VLSI Technology	3	0	0	3
4.	EC6204	Analog Integrated Circuit Design	3	0	0	3
5.		Elective 1	3	0	0	3
6.	EC6205	Micro Electronic Lab I	0	0	3	2
7.	EC6206	System Design Using HDL	0	0	3	2
		Total credits				20

Semester 2

S. No.	Code	Name of the Subject	L	T	P/S	C
1.	EC6207	MOS Device Modeling	3	0	0	3
2.	EC6208	VLSI System Design	3	0	0	3
3.		Elective 1	3	0	0	3
4.		Elective 2	3	0	0	3
5.		Elective 3	3	0	0	3
6.	EC6209	Micro Electronic Lab II	0	0	3	2
7.	EC6210	VLSI Design Lab	0	0	3	2
8.	EC6211	Seminar	0	0	2	1
		Total credits				20

Semester 3

S. No.	Code	Name of the Subject	L	T	P/S	C
1.	EC7201	Project Work	-	-	-	8
		Total credits				8

Semester 4

S. No.	Code	Name of the Subject	L	T	P/S	C
1.	EC7202	Project Work	-	-	-	12
		Total credits				12

Minimum Requirements

Minimum number of credits to be earned by a student is 60

List of Electives

S.No.	Code	Name of the Subject	L	T	P/S	C
1.	EC6221	Compound Semiconductors: Properties & Applications	3	0	0	3
2.	EC6222	Micro Electro Mechanical Systems	3	0	0	3
3.	EC6223	Foundation of VLSI CAD	3	0	0	3
4.	EC6224	Testing & Verification of VLSI Circuits	3	0	0	3
5.	EC6225	Semiconductor Power Devices	3	0	0	3
6.	EC6226	Nanoelectronics	3	0	0	3
7.	EC6227	Low Power VLSI	3	0	0	3
8.	EC6228	Mixed Signal circuit design	3	0	0	3
9.	EC6229	Selected topics in circuits design	3	0	0	3
9.	EC6230	CMOS RF circuit design	3	0	0	3

*Any other subject (core/elective) offered by the Department from time to time shall be taken as elective with the consent of course co-ordinator/faculty.

Syllabus of M. Tech. Degree Programme in Microelectronics and VLSI Design

SEMESTER-I

EC6201: Basics of VLSI

Pre-requisites: -NIL-

L	T	P/S	C
3	0	3	4

Course Outcomes :

- ***CO1****: Calculate various parameters of a MOSFET*
- ***CO2****: Explain various short channel effects and explain their effects on circuit performance*
- ***CO3****: Ability to design Transistor-Level CMOS Logic circuit for a given functionality*
- ***CO4****: An ability to estimate timing characteristics, noise margins, power consumption of a digital VLSI circuit.*
- ***CO5****:Analyze Gate Function and Timing Characteristics of a multi input CMOS Logic gates*
- ***CO6****:Estimate timing of a complex VLSI circuit using Logical Effort analysis.*
- ***CO7****:To identify reasons for delay in a VLSI gate/circuit and apply various techniques to reduce delay of gate/circuit.*
- ***CO8****:Design static CMOS and dynamic clocked CMOS circuits.*
- ***CO9****:Draw layout of a CMOS circuit*
- ***CO10****:Identify and explain the role of parasitic elements in a CMOS digital circuit*
- ***CO11****:To compare various logic design styles on their performance metrics (speed, power consumption, area:*
- ***CO12****:Analyze working of SRAM cell and DRAM cell*

Total Hours 42 Hrs Theory + 42 Hrs Lab

Module 1 (11 hours)

Introduction MOSFET, threshold voltage, current, Channel length modulation, body bias effect and short channel effects, MOS switch, MOSFET capacitances, MOSFET models for calculation-Transistors and Layout, CMOS layout elements, parasitics, wires and vias-design rules-layout design SPICE simulation of MOSFET I-V characteristics and parameter extraction

Module 2 (10 hours)

CMOS inverter, static characteristics, noise margin, effect of process variation, supply scaling, dynamic characteristics, inverter design for a given VTC and speed, effect of input rise time and fall time, static and dynamic power dissipation, energy & power delay product, sizing chain of inverters, latch up effect-Simulation of static and dynamic characteristics, layout, post layout simulation

Module 3 (13 hours)

Static CMOS design, Complementary CMOS, static properties, propagation delay, Elmore delay model, power consumption, low power design techniques, logical effort for transistor sizing, ratioed logic, pseudo NMOS inverter, DCVSL, PTL, DPTL & Transmission gate logic, dynamic CMOS design, speed and power considerations, Domino logic and its derivatives, C2MOS, TSPC registers, NORA CMOS – Course project

Module 4 (8 hours)

Circuit design considerations of Arithmetic circuits, shifter, CMOS memory design - SRAM and DRAM, BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic

References:

1. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis & Design, , MGH, Third Ed., 2003

2. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective,Prentice Hall, Second Edition, 2005

3. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Analysis and Design of Digital Integrated Circuits, Third Edition, McGraw-Hill, 2004

4. R. J. Baker, H. W. Li, and D. E. Boyce, CMOS circuit design, layout, and simulation, Wiley-IEEE Press, 2007

5. Christopher Saint and Judy Saint, IC layout basics: A practical guide, McGraw-Hill Professional, 2001

EC6202: Semiconductor Device Theory and Modelling

Pre-requisites: : -NIL-

L	T	P/S	C
3	0	0	3

Course Outcomes:

- ***CO1****: Explain the need of quantum mechanics in semiconductor design*
- ***CO2****:Compute carrier electronic properties in semiconductor materials and devices under different operating conditions.*
- ***CO3****:Draw band diagram of different semiconductor devices under different bias conditions*
- ***CO4****:Apply suitable approximations and techniques to derive the model referred to above starting from drift-diffusion transport equations*
- ***CO5****:Compute electrostatic variables and current-voltage characteristics of semiconductor devices under a variety of conditions.*
- ***CO6:****To design a pn junction device and bi-polar devices as per requirements*
- ***CO7****:Explain and compute figures of merit of bipolar device based on device parameters and dimensions*
- ***CO8****: Explain various non ideal effects in a bipolar transistor*
- ***CO9:****To provide qualitative understanding of the physics of a new device and conversion of this understanding into equations*

Total Hours: 42 Hrs.

Module 1 (16 hours)

Review of quantum mechanics, Electrons in potentials (infinite barrier, potential well), Electrons in periodic lattices (KP Model), E-k diagrams, effective mass; Quasi-particles in semiconductors, electrons, holes (light holes and heavy holes), optical and acoustic phonons, electron hole pair (EHP). Band diagram of silicon, intrinsic and extrinsic carrier concentration, relation between applied voltage and Fermi level, Carrier statistics; Generation-recombination, SRH theory, diffusion length, carrier life time, Continuity equation, Poisson's equation and solution, Boltzmann transport equation, Mobility and diffusivity; variation of mobility with temperature, doping, high filed mobility, low field mobility, Hall mobility/Hall experiment, sheet resistance, drift and diffusion.

Module 2 (14 hours)

Junction devices- PN junction diode: band diagrams, electrostatics of a pn junction diode, CV characteristics, IV characteristics, high level injection, low level injection, ac characteristics: admittance of a diode, break down phenomenon in diodes; MS contact, band diagrams, ohmic and non ohmic contacts, thermionic Emission model for current transport and current-voltage

(I-V) characteristics, effect of interface states and interfacial thin electric layer on the Schottky barrier height and the I-V characteristics; Solar cells

Module 3 (12 hours)

Bipolar Junction Transistors (12 hours): Structure of a BJT, carrier statistics in base, emitter, collector, figures of merit, basic principle of operation, long base transistor, short base transistor, analysis of ideal diffusion transistor, Ebers-Moll model, narrow base effects, narrow emitter effects, current crowding, effect of narrow base width and emitter width on device figures of merit, high level injection effects, Kirk effect, BJT at high frequencies

References:

1. M.S.Tyagi, John, Introduction to Semiconductor materials and Devices, Wiley & Sons, ISBN: 9971-51-316-1
2. Donald A Neamen, Semiconductor Physics and Devices: Basic Principles, McGraw-Hill (1997) ISBN 0-256-24214-3
3. Ben G. Streetman (2000), Solid State Electronic Devices, 5th Edition, ISBN 0-13-025706-0
4. S.M. Sze, Modern Semiconductor Device Physics, Wiley (1998) ISBN 0-471-15237-4
5. Robert F. Pierret, Semiconductor Device Fundamentals, Addison-Wesley (1995), ISBN 020154393-1, (Indian edition available)
6. J.P.Colinge, C.A.Colinge, Physics of Semiconductor Devices, Kulwer Academic Publishers, ISBN 1-40207-018-7 (available online at NITC intranet, in Springer eBook library, status 15th March 2010)
7. Yuan Taur & Tak H Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 1998.
8. S M Sze, High speed semiconductor devices, John Wiley, 1990
9. BRENNAN, Kevin F, Introduction to semiconductor devices: for computing and telecommunications applications, Cambridge Press, London, 2005, ISBN 978-0-521-67036-4.
10. KANO Kanaan, Semiconductor devices, Prentice hall: New Delhi, 1998, ISBN 8131705358.

EC6203: VLSI Technology

Pre-requisites: -NIL-

L	T	P/S	C
3	0	0	3

Course Outcomes :

- ***CO1:****Understand the material properties, crystalline structure of silicon and different crystal growth techniques.*
- ***CO2:****Kinetics of Silicon dioxide growth both for thick, thin and ultra thin films and oxidation modeling*
- ***CO3:****Techniques for introducing dopants into the bulk material , comparison of diffusion and ion implantation, modeling*
- ***CO4:****Deposition Techniques, Importance of High k and Low k dielectrics*
- ***CO5:****Etching, photolithography and metallization methods*

Total Hours: 42 Hrs.

Module 1 (6 hours)

Material properties, crystal structure, lattice, basis, planes, directions, angle between different planes, characterization of material based on band diagram and bonding, conductivity, resistivity, sheet resistance, phase diagram and solid solubility, Crystal growth techniques, wafer cleaning, Epitaxy, Clean room and safety requirements.

Module 2 (17 hours)

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultra thin films, Deal-Grove model and Improvements in Deal-Grove method for thin and ultra thin oxide layers, thickness characterization methods, multi dimension oxidation modelling.

Diffusion and Ion Implantation: Diffusion process, Solid state diffusion modeling, various doping techniques, Ion implantation, modeling of Ion implantation, statistics of ion implantation, damage annealing, thermal budget, rapid thermal annealing, spike anneal, advanced annealing methods, Implant characterization SIMS, spreading resistance method.

Deposition & Growth: Various deposition techniques CVD, PVD, evaporation, sputtering, spin coating, LPCVD, epitaxy, MBE, ALCVD, Growth of High k and low k dielectrics

Module 3 (13 hours)

Etch and Cleaning: materials used in cleaning, various cleaning methods, Wet etch, Dry etch, Plasma etching, RIE etching, etch selectivity/selective etch.

Photolithography: Positive photo resist, negative photo resist, comparison of photo resists, components of a resist, light sources, exposure, Resolution, Depth of Focus, Numerical Aperture (NA), sensitivity, contrast, need for different light sources, masks, Contact, proximity and projection lithography, step and scan, optical proximity correction, develop(development

of resist), Next generation technologies: Immersion lithography, Phase shift mask, EUV lithography, X-ray lithography, e-beam lithography, ion lithography, SCALPEL.
Planarization Techniques: Need for planarization, Chemical Mechanical Polishing

Module 4 (6 hours)
Copper damascene process, Metal interconnects; Multi-level metallization schemes, Process integration: NMOS, CMOS and Bipolar process.

References:
1. James Plummer, M. Deal and P.Griffin, Silicon VLSI Technology, Prentice Hall Electronics
2. Stephen Campbell, The Science and Engineering of Microelectronics, Oxford University Press, 1996
3. S.M. Sze (Ed), VLSI Technology, 2nd Edition, McGraw Hill, 1988
4. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1983.
5. C.Y. Chang and S.M.Sze (Ed), ULSI Technology, McGraw Hill Companies Inc, 1996.

EC6204: Analog Integrated Circuit Design

Pre-requisites: **-**NIL-

L	T	P/S	C
3	0	0	3

Course Outcomes:

- ***CO1:****Understanding the small signal models and approximations for analog circuit analysis and design*
- ***CO2:****Understanding the bias variations under environmental, circuit non-idealities and designing suitable biasing for a given circuit*
- ***CO3:****Understanding single stage amplifiers and designing amplifiers for given specifications*
- ***CO4:****Formulating design procedures of one and two stage operational amplifiers and designing them using CAD tools for open loop and feedback applications*
- ***CO5:****Understanding the role of feedback on oscillation and different oscillator configurations*

Total Hours: 42 Hrs.

Module 1 (12 hours)

Introduction MOSFET, threshold voltage, current, Channel length modulation, body bias effect-MOSFET models in saturation, linear and cutoff regions-current sources and sinks - current mirrors - cascode, Wilson current mirrors - voltage references - Supply independent and temperature independent references - Band gap references.

Module 2 (10 hours)

Common source with resistive, diode connected, current source and triode loads, CS with source degeneration, common gate and source follower stages- 14ascade and folded 14ascade structures- frequency response of CS, CD and CG configurations – noise in single stage amplifiers.

Module 3 (13 hours)

MOS differential amplifiers – common mode response – differential pair with MOS loads – Noise in differential pair-CMOS operational amplifiers - One-stage op-amps and two stage op-amps –gain boosting – Miller,Nulling resistor compensation.

Module 4 (7 hours)

CMOS oscillators - ring oscillators - LC oscillators – colpitts and one-port oscillators – voltage controlled oscillators – tuning in oscillators.

References:

1. David A Johns & Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons, 2001.

2. Behzad Razavi, Design of Analog CMOS Integrated Circuit, Tata-Mc GrawHill, 2002.

3. Philip Allen & Douglas Holberg, CMOS Analog Circuit Design, Oxford University Press, 2002.

EC6205: Micro Electronics Lab I

Pre-requisites: -NIL-

L	T	P/S	C
0	0	3	2

Course Outcomes:

- ***CO1:*** *Familiarize the process and device simulator tools*
- ***CO2:*** *Simulate (2D) the characteristics of p-n junction diodes using the device simulator*
- ***CO3:*** *2D simulation of Bipolar junction transistors using the device simulator*
- ***CO4:*** *2D simulations of diode process and BJT process using 2D process simulator*
- ***CO5:*** *3D simulation of diodes using 3D device simulator*

Total Hours 28 Hrs.

Note: The experiments are planned in such a way that EC6205 complements EC6202 and EC6203

Familiarization of Simulator:
Know how of gridding techniques (adaptive gridding), various modules in the simulator (process module (2D & 3D), device module (2D & 3D), mixed mode module etc.), information on models. In doing so a simple experiment as described below may be planned.
Note: It is expected that students will spend some time outside the lab hours to know more on different models.

PN diode simulations:
2D simulations (4 sessions): Use device simulator to generate a pn diode structure. Simulate I-V characteristics and also get the C-V characteristics. Find the carrier concentration, electron and hole concentration, electric field, potential distribution (at different biases) and doping distribution across the structure. Check the current and capacitance values with hand calculations. Extract V_{bi} from capacitance characteristics. Freeze different models one used. Process simulate the same structure with same/similar doping levels. Exporting the process simulated structure in to device simulator, extract I-V

and C-V characteristics and make similar observations as in device simulation and explain the differences if any.

3D simulations (2 sessions): The effect of series resistance is very important and most of the times a series resistance is what determines the current through pn diode. This experiment aims to simulate such an effect (no need a mixed mode simulator). Study the effect of series the on current through the device with change in series resistance.

BJT simulations:

2D simulations (3 sessions): Bipolar devices are very important devices to understand. Any given MOSFET has a parasitic BJT. If not taken care in device design, the parasitic BJT may lead to very different behavior. The aim of these experiments is to understand the different effects in BJT. For a lateral/planar BJT, the following experiments can be performed:

1) Variation in α, β_{dc} and γ with base doping and base width and respective current characteristics

2) Variation α, β_{dc} and γ with emitter width and respective current characteristics

3D simulations (2 sessions): For a Vertical BJT effect of poly emitter on device performance, carrier concentration, electron and hole concentration, potential and electric field distributions across the BJT, impact ionization.

References:

1. User manuals of software used in the labs.

2. Donald A Neamen, Semiconductor Physics and Devices: Basic Principles, McGraw-Hill (1997) ISBN 0-256-24214-3.

3. Ben G. Streetman, Solid State Electronic Devices, 5th Edition, (2000), ISBN 0-13-025706-0.

4. S.M. Sze, Modern Semiconductor Device Physics, Wiley (1998) ISBN 0-471-15237-4.

5.Robert F. Pierret, Semiconductor Device Fundamentals, Addison-Wesley (1995), ISBN 020154393-1, (Indian edition available).

6. J.P. Colinge, C.A. Colinge, Physics of Semiconductor Devices, Kulwer Academic Publishers, ISBN 1-40207-018-7 (available online at NITC intranet, in Springer eBook library, status 15th March 2010).

7. M.S.Tyagi, Introduction to Semiconductor materials and Devices, John Wiley & Sons, ISBN: 9971-51-316-1.

EC6206: System Design Using HDL

Pre-requisites: -NIL-

L	T	P/S	C
0	0	3	2

Course Outcomes:

- ***CO1:*** *Develop the ability to use industry standard tools to design, simulate and verify digital logic circuits and systems.*
- ***CO2:*** *Learn to design combinational and sequential circuits.*
- ***CO3:*** *Learn to practice standard design flow and handle FPGA development boards for prototyping digital systems.*
- ***CO4:*** *Learn to debug the design flaws using software tools and address critical design issues.*
- ***CO5:*** *Develop the ability to work as team to design a digital system and demonstrate it by using FPGA development board, oral presentation and document it by well written report.*

Total Hours : 42 Hrs.

1. Combinational logic using HDL gate models.
2. HDL models for flip flops, multiplexers and memory.
3. HDL models of sequential logic blocks.
4. Test benches for combinational and sequential blocks.
5. State machines.
6. Simulation techniques.
7. RTL synthesis and synthesis for FPGA.
8. Mapping, place & route.
9. Constraints and debugging.
10. Interfacing with on board I/O.
11. Interfacing with external system.
12. Course project.

References:

1. Mark Zwolinski, Digital System Design with VHDL, Pearson education, 2004.
2. Charles H Roth Jr., Digital System Design using VHDL, Thomson Brooks/Cole,2006.

SEMESTER-II

EC6207: MOS Device Modelling

Pre-requisites: EC6202 or equivalent

L	T	P/S	C
3	0	0	3

Course Outcomes :

- ***CO1****:Explain the underlying physics and principles of operation of Metal-Oxide-Semiconductor devices*
- ***CO2:*** *Explain and compute capacitance-voltage characteristics of a MOC capacitor*
- ***CO3****: Derive and compute threshold voltage, and current-voltagecharacteristics, of a MOS field effect transistor.*
- ***CO4****: Explain different Short Channel Effects and their effect on device and circuit performance.*
- ***CO5****: Explain Drain and Channel Engineering including hot carrier effects, latch-up and breakdown.*
- ***CO6****: Derive various MOSFET Models that are used in mathematical calculations and simulation.*
- ***CO7****: Derive small signal circuit models at low frequency and high frequency.*
- ***CO8****: Derive various MOSFET Models that are used in mathematical calculations and simulation.*
- ***CO9****: Explain various effects associated with SOI MOSFETs.*
- ***CO10****: Explain working of new device structures and materials*

Total Hours: 42 Hrs.

Module 1 (13 hours)

Semiconductor surfaces, Ideal MOS structure, MOS device in thermal equilibrium, Non-Ideal MOS: work function differences, charges in oxide, interface states, band diagram of non ideal MOS, flatband voltage, electrostatics of a MOS (charge based calculations), calculating various charges across the MOSC, threshold voltage, MOS as a capacitor (2 terminal device), Three terminal MOS, effect on threshold voltage.

Module 2 (10 hours)

MOSFET (Enhancement and Depletion MOSFETs), mobility, on current characteristics, off current characteristics, sub threhsold swing, effect of interface states on sub threshold swing, drain conductance and transconductance, effect of source bias and body bias on threshold voltage and device operation.

Module 3 (6 hours)
Scaling, Short channel and narrow channel effects- High field effects.

Module 4 (5 hours)
MOS transistor in dynamic operation, Large signal Modeling, small signal model for low, medium and high frequencies.

Module 5 (8 hours)
SOI concept, PD SOI, FD SOI and their characteristics, threshold voltage of a SOI MOSFET, Multi-gate SOI MOSFETs, Alternate MOS structures.

References:
1. E.H. Nicollian, J. R. Brews, Metal Oxide Semiconductor - Physics and Technology, John Wiley and Sons.
2. Nandita Das Guptha, Amitava Das Guptha, Semiconductor Devices Modeling and Technology, Prentice Hall India
3. Jean- Pierrie Colinge, Silicon-on-insulator Technology: Materials to VLSI, Kluwer Academic publishers group.
4. Yannis Tsividis, Operation and Modeling of the MOS transistor, Oxford University Press.
5. M.S.Tyagi, Introduction to Semiconductor materials and Devices, John Wiley & Sons, ISBN: 9971-51-316-1.
6. Donald A Neamen, Semiconductor Physics and Devices Basic Principles, McGraw-Hill (1997) ISBN 0-256-24214-3.
7. S.M. Sze, Modern Semiconductor Device Physics, Wiley (1998) ISBN 0-471-15237-4.
8. Robert F. Pierret, Semiconductor Device Fundamentals, Addison-Wesley (1995), ISBN 020154393-1, (Indian edition available).
9. J.P.Colinge, C.A.Colinge, Physics of Semiconductor Devices, Kulwer Academic Publishers, ISBN 1-40207-018-7 (available online at NITC intranet, in Springer eBook library, status 15th March 2010).
10. Yuan Taur & Tak H Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 1998.
11. BRENNAN, Kevin F, Introduction to semiconductor devices: for computing and telecommunications applications, Cambridge Press, London, 2005, ISBN 978-0-521-67036-4.
12. KANO, Kanaan, Semiconductor devices, Prentice hall: New Delhi, 1998, ISBN 8131705358.
13. Christaian C. Enz, Cric A. Vittoz, Charge-based MOS Transistor Modeling, John Wiley 2006, ISBN-0-479-85541-X
14.A.B.Bharracharya, Compact MOSFET Models for VLSI Design, John Wiley 2009, ISBN 978-0-470-82342-2.

EC6208: VLSI System Design

Pre-requisites: EC6201

L	T	P/S	C
3	0	0	3

Course Outcomes:

- ***CO1:*** *Understand the custom and semi custom digital IC design flow in VLSI.*
- ***CO2:*** *Understand the concept of logic synthesis, optimization, scheduling and resource allocation and learn how to apply these to multi million gate designs.*
- ***CO3:*** *Learn to design a digital system without any timing issues by understanding the problems associated with such systems like slack, skew, jitter and interconnect noises.*
- ***CO4:*** *Understand the backend design processes such as partitioning, floorplaning, placement and routing by learning the various classical algorithms developed for these purposes and develop the ability to solve the new problems associated with miniaturization of VLSI circuits.*
- ***CO5:*** *Learn the system design using reconfigurable architectures and the design flow followed as well as the critical design issues.*
- ***CO6:*** *Develop the ability to work as team to design a digital system and demonstrate it by giving oral presentation and document it by well written report*.

Total Hours: 42 Hrs.

Module 1 (11 hrs)

Introduction to digital IC design – Custom and semicustom flow, combinational logic synthesis – Technology independent and technology dependent optimization –Logic synthesis -High level synthesis- Scheduling and allocation-ASAP and ALAP scheduling-Register allocation-Functional unit allocation-Interconnect path allocation-Hardware description languages-synthesis-register transfer design-Event driven simulation.

Module 2 (11 hrs)

Subsystem design principles-pipelining-Data paths in processor architecture – Standard cell layout-Logic design considerations of adder and multiplier- Timing -Slack delay model – Effect of skew and jitter on timing, Sources of skew and jitter- Clocking disciplines -Wire model-Technology scaling effect on interconnect and -Noise in interconnects.

Module 3 (11 hrs)

Partitioning-Floorplanning and pin assignment-Slicing tree –Channel definition-Channel routing order-Wind mill constraint-Placement-Special routing-Clock routing for regular and irregular

structures-Power routing-Global routing-Line Probe algorithm-Maze routing-Detail routing-Left edge algorithm-Vertical constraint-switch box routing.

Module 4 (9 hrs)
FPGA logic element and interconnect architecture-logic synthesis for FPGA-Physical design for FPGA-I/O circuits, ESD protection, Off chip connections.

References:
1. James R.Armstrong, F.Gail Gray, VHDL Design Representation and Synthesis, Pearson education, 2007.
2. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, Prentice Hall, Second Edition, 2005.
3. Wayne Wolf, FPGA-Based System Design, Pearson, 2009.
4. Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation, Springer,Third edition,1999.

EC6209: Micro Electronics Lab II

Pre-requisites: -NIL-

L	T	P/S	C
0	0	3	2

Course Outcomes:

- ***CO1:*** *Simulate MOS capacitor and obtain CV characteristics.*
- ***CO2:*** *Simulate of long channel MOSFET to obtain IV characteristics*
- ***CO3:*** *Simulation of threshold voltage roll off of short channel MOSFETs*
- ***CO4:*** *simulation of novel MOSFET structures*

Total Hours: 42 Hrs.

The experiments are planned in such a way that EC6209 complements EC6207.

1) Simulate C-V characteristics of a MOS capacitor with a poly silicon gate. Here you need two different structures. One structure should be suitable for a long channel devices, meaning the oxide thickness, substrate doping etc. should be used to simulate long channel devices in (2). Second structure should be suitable for simulating short channel devices in (3). Note the

flatband and threshold voltages. Is there any difference in the observed gate capacitance value in inversion? If so, what could be the reason? **(1-2 sessions)**

2) Long channel MOSFET device simulations to familiarize different device models. Find current characteristics and various conductance values. Is there any difference in the threshold voltage values? **(2 sessions)**

3) Process simulation of a MOSFET (please refer to ITRS roadmap for a suitable device geometries. oxide capacitance and substrate doping should be same as short channel device in (1)). Note doping distribution, carrier concentration, field and potential distributions across the device (2 sessions). Compare the threshold voltage values with the capacitor in (1). If the values are different, what could be the reason? How one can increase the threshold voltage, implement in the process and device simulation. **(3 sessions)**

4) Use the structure generated in (3) to perform device simulations and extract various device parameters. **(1 session)**

5) Simulate a 3D MOS device (FINFET/SOI/Piller MOSFET) and obtain their characteristics. **(3 sessions)**

References:

1. E.H. Nicollian, J. R. Brews, Metal Oxide Semiconductor - Physics and Technology, John Wiley and Sons.
2. User Manuals of respective software.
3. Jean- Pierrie Colinge, Silicon-on-insulator Technology: Materials to VLSI, Kluwer Academic publishers group.
4. Yannis Tsividis, Operation and Modeling of the MOS transistor, Oxford University Press.
5. M.S. Tyagi, Introduction to Semiconductor materials and Devices, John Wiley & Sons, ISBN: 9971-51-316-1.

EC6210: VLSI Design Lab

Pre-requisites: -NIL-

L	T	P/S	C
0	0	3	2

Course Outcomes:

- ***CO1:****Develop the ability to understand the basic principles of VLSI circuit design and examine the basic building blocks of very large scale digital integrated circuits and provide hands-on design experience with professional Electronic Design Automation (EDA) tools*
- ***CO2:****Learn to do synthesis by applying suitable constraints and get the circuit matching the specification.*
- ***CO3:****Learn to practice standard ASIC design flow and convert the RTL to GDS format through standard procedures like floorplanning, placement, routing, parasitic extraction, post layout simulation, etc.,*
- ***CO4:****Learn to debug the design flaws using software tools and address critical design issues at various stages of the design flow.*
- ***CO5:*** *Develop the ability to work as team and design ASIC digital system from RTL to GDS demonstrate it by oral presentation and document it by well written report*.

Total Hours: 42 Hrs.

1. Synthesis with timing constraints
2. Clock tree synthesis
3. Low power synthesis
4. Pre layout simulation
5. Floorplanning
6. Placement
7. Routing
8. Parasitic extraction
9. Post layout simulation
10. Standard cell layout

References:

1. James R.Armstrong, F.Gail Gray, VHDL Design Representation and Synthesis, Pearson education, 2007.
2. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, Prentice Hall, Second Edition, 2005.
3. Wayne Wolf, FPGA-Based System Design, Pearson, 2009.
4. Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation, Springer, Third edition,1999.

EC6211: Seminar

Pre-requisites: -NIL-

L	T	P/S	C
0	0	2	1

Course Outcomes:

- ***CO1****:Student will get exposure to the recent technical advancements.*
- ***CO2****:Student will explore and engage in higher order thinking activities related to a recent topic from their academic area.*
- ***CO3****:Student learns to acquire the materials, articulate, create and convey intended meaning of their topics effectively.*
- ***CO4****:Student learns to express themselves clearly and persuasively in exposition and in argument.*
- ***CO5****: Student will practice oral and written communication skills.*

SEMESTER-III

EC7201: PROJECT WORK

L	T	P/S	C
0	0	0	8

Course Outcomes:

- ***CO1****: Identify research problems in the broad area of Microelectronics and VLSI Design for research*
- ***CO2****: Generate, organize and interpret data, and draw conclusions*
- ***CO3****: Develop new models/products which will improve the technology and/ beneficial to the society.*
- ***CO4****: Learn to use modern tools effectively*
- ***CO5****: Develop oral and /written communication skills.*

- ***CO6****: Develop critical thinking, self learning and creativity of students .*
- ***CO7*** *: Practise professionalism and ethics.*

Syllabus:

The student will be encouraged to fix the area of the project work and conduct the literature review towards the end of second semester. The project work starts in the third semester. The topic shall be research and development oriented in the emerging areas of Communication/ allied fields, under the supervision of a faculty from the ECE Department. The project can be carried out at the institute or in an industry/research organization. (Students desirous of carrying out project in industry or other organization have to fulfill the requirements as specified in the "Ordinances and Regulations for M. Tech.").

The students are supposed to complete a good quantum of the work in the third semester. There shall be evaluation of the work carried out in the third semester by the PG evaluation committee constituted by the department for Communication Stream. The project work started in the third semester will be extended to the end of the fourth semester. There shall be evaluations of the project work by the committee and by an external examiner during and at the end of fourth semester.

SEMESTER-IV

EC7202: PROJECT WORK

L	T	P/S	C
0	0	0	12

See EC 7201

LIST OF ELECTIVES

EC6221: Compound Semiconductors: Properties & Applications

Pre-requisites: EC6202

L	T	P/S	C
3	0	0	3

Course Outcomes:

- ***CO1:*** *Understand Important parameters governing the high speed performance of devices and circuits*
- ***CO2:*** *Understand the properties of Heterojunctions from the energy band diagram point of view*
- ***CO3*** *Study the operation and modelling of Hetero junction Bipolar Transistor*
- ***CO5:*** *Understand the operation of tunnelling devices and Hot electron Devices,*
- ***CO4:*** *Study the operation and modelling of Hetero junction Bipolar Transistor*

Total Hours: 42 Hrs.

Module 1 (6 hours)

Important parameters governing the high speed performance of devices and circuits: Transit time of charge carriers, junction capacitances, ON-resistances and their dependence on the device geometry and size, carrier mobility, doping concentration and temperature; important parameters governing the high power performance of devices and circuits: Break down voltage, resistances, device geometries, doping concentration and temperature.

Module 2 (16 hours)

Materials properties: Merits of III –V binary and ternary compound semiconductors (GaAs, InP, InGaAs, AlGaAs, SiC, GaN etc.), different SiC structures, silicon-germanium alloys and silicon carbide for high speed devices, as compared to silicon based devices, outline of the crystal structure, dopants and electrical properties such as carrier mobility, velocity versus electric field characteristics of these materials, electric field characteristics of materials and device processing techniques, Band diagrams, homo and hetro junctions, electrostatic calculations, Band gap engineering, doping, Material and device process technique with these III-V and IV – IV semiconductors.

Module 3 (8 hours)

Metal semiconductor contacts and Metal Insulator Semiconductor and MOS devices: Native oxides of Compound semiconductors for MOS devices and the interface state density related issues. Metal semiconductor contacts, Schottky barrier diode, Metal semiconductor Field Effect

Transistors (MESFETs): Pinch off voltage and threshold voltage of MESFETs. D.C. characteristics and analysis of drain current. Velocity overshoot effects and the related advantages of GaAs, InP and GaN based devices for high speed operation. Sub threshold characteristics, short channel effects and the performance of scaled down devices.

Module 4 (12 hours)

High Electron Mobility Transistors (HEMT): Hetero-junction devices. The generic Modulation Doped FET(MODFET) structure for high electron mobility realization. Principle of operation and the unique features of HEMT, InGaAs/InP HEMT structures: Hetero junction Bipolar transistors (HBTs): Principle of operation and the benefits of hetero junction BJT for high speed applications. GaAs and InP based HBT device structure and the surface passivation for stable high gain high frequency performance. SiGe HBTs and the concept of strained layer devices; High Frequency resonant – tunneling devices, Resonant-tunneling hot electron transistors

References:

1. C.Y. Chang, F. Kai, GaAs High-Speed Devices: Physics, Technology and Circuit Applications, Wiley & Sons.
2. Cheng T. Wang, Ed., Introduction to Semiconductor Technology: GaAs and Related Compounds, John Wiley & Sons.
3. David K. Ferry, Ed., Gallium Arsenide Technology, Howard W. Sams & Co., 1985
4. Avishay Katz, Indium Phosphide and Related materials: Processing, Technology and Devices, Artech House, 1992.
5. S.M. Sze, High Speed Semiconductor Devices, Wiley (1990) ISBN 0-471-62307-5
6. Ralph E. Williams, Modern GaAs Processing Methods, Artech (1990), ISBN 0-89006-343-5,
7. Sandip Tiwari, Compound Semiconductor Device Physics, Academic Press (1991), ISBN 0-12-691740-X.
8. G.A. Armstrong, C.K. Maiti, TCAD for Si, SiGe and GaAs Integrated Circuits, The Institution of Engineering and Technology, London, United Kingdom, 2007,ISBN 978-0-86341-743-6.
9. Ruediger Quay, Gallium Nitride Electronics, Springer 2008, ISBN 978-3-540-71890-1, (Available on NITC intranet in Springer eBook section).
10. Prof. Dr. Alessandro Birolini, Reliability Engineering Theory and Practice, Springer 2007, ISBN-10 3-540-40287-X, Available on NITC intranet in Springer eBook section).

EC6222: Micro Electro Mechanical Systems

Pre-requisites: -NIL-

L	T	P/S	C
3	0	0	3

Course Outcomes :

- ***CO1:*** *An introduction to microsensors and actuators and different applications in MEMS.*
- ***CO2:*** *Different micromachining technologies in MEMS*
- ***CO3:*** *Introduction on micromachined microsensors and their different types*
- ***CO4:*** *MEMS Simulators and different FEA tools*
- ***CO5:*** *Bonding and Packaging of MEMS*

Total Hours: 42 Hrs.

Module 1 (6 Hours)
An introduction to Micro sensors and MEMS, Evolution of Micro sensors & MEMS, Micro sensors & MEMS applications

Module 2 (12 Hours)
Microelectronic technologies for MEMS, Micromachining Technology, Surface and Bulk Micromachining, working principle of various MEMS.

Module 3 (12 Hours)
Micro machined Micro sensors: Mechanical, Inertial, Biological, Chemical, Acoustic, Microsystems Technology, Integrated Smart Sensors and MEMS.

Module 4 (12 hours)
Interface Electronics for MEMS, MEMS Simulators, MEMS for RF Applications, Bonding & Packaging of MEMS, Conclusions & Future Trends.

References:
1. Tai-ran Su, MEMS and Microsystems: design and Manufacture, Tata McGraw Hill.
2. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1983.
3. S.M. Sze (Ed), VLSI Technology, McGraw Hill, 1988.
4. Julian W. Gardner, V. K. Varadan, Osama O. Awadelkarim, Microsensors, MEMS, and Smart Devices, ISBN: 047186109X - John Wiley and Sons.
5. Gere & Timoshenko, Mechanics of Materials, PWS-KENT, 1990.
6.Gregory T. A. Kovacs, Micromachined Transducers Sourcebook, WGB/McGraw-Hill,2000, ISBN: 0072907223.

7. M. Madou, Fundamentals of Microfabrication, CRC Press, 2002, ISBN: 0849308267
8. M. Elwenspoek & H. Jansen, Silicon micromachining, Cambridge, 1998, ISBN: 052159054
9. S. Senturia, Microsystem Design, Kluwer Academic Publishers, 2001, ISBN: 0792372468
10. S.Sze, Semiconductor Sensors, John Wiley & Sons, 1994 ISBN: 0471546097
11. Marc Madou, Fundamentals of Microfabrication, CRC Press, 1997.
12. Edited by William S. Trimmer, Micromechanics and MEMs, IEEE Press, 1997.
13. Edited by Richard S. Muller,Microsensors, IEEE Press, 1991.
14.Editor P.Rai-Choudhury, Handbook of Microlithography, Micromachining, and Microfabrication, SPIE-The International Society for Optical Engineering, 1997.
15. "Journal of Microelectromechanical Systems", Joint IEEE/ASME Publication.
16. Kovacs, Micromachined Transducers, McGraw Hill.

EC6223: Foundations Of VLSI CAD

Pre-requisites: **-**NIL-

L	T	P/S	C
3	0	0	3

Course Outcomes:

- ***CO1:*** *Solving CAD problems using algorithms and data structures*
- ***CO2:*** *Identifying suitable type of data structure for a graph*
- ***CO3:*** *Representing graphs using matrices*
- ***CO4:*** *Understanding vector spaces and solution spaces for linear equations*
- ***CO5:*** *Estimating complexity of an algorithm*

Total Hours: 42 Hrs.

Module 1 (10 hours)
Matrices: Linear dependence of vectors, solution of linear equations, bases of vector spaces, orthogonality, complementary orthogonal spaces and solution spaces of linear equations.

Module 2 (12 hours)
Graphs: representation of graphs using matrices; Paths, connectedness; circuits, cutsets, trees; Fundamental circuit and cutset matrices; Voltage and current spaces of a directed graph and their complementary orthogonality.

Module 3 (12 hours)

Algorithms data structures: efficient representation of graphs; Elementary graph algorithms involving bfs and dfs trees, such as finding connected and 2- connected components of a graph, the minimum spanning tree, shortest path between a pair of vertices in a graph

Module 4 (8 hours)
Data structures such as stacks, linked lists and queues, binary trees and heaps. Time and space complexity of algorithms

References:
1. K. Hoffman and R.E. Kunze, Linear Algebra, Prentice Hall (India), 1986
2.N.Balabanian and T.A. Bickart, Linear Network Theory: Analysis, Properties, Design and Synthesis, Matrix Publishers, Inc., 1981.
3. T.Cormen, C.Leiserson and R.A.Rivest, Algorithms, MIT Press and McGraw-Hill, 1990.
4. Neil H. E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Second Edition, Addison Wesley, 1993.
5. Neil H. E. Weste and David Harris, Principles of CMOS VLSI Design, Third Edition, Addison Wesley, 2004.

EC6224: Testing and Verification of VLSI Circuits

Pre-requisites: An undergraduate or first level post graduate course in Digital IC Design

L	T	P/S	C
3	0	0	3

Course Outcomes:

- ***CO1:****Model different types of faults in the digital circuits using appropriate fault models.*
- ***CO2:*** *Generate test patterns required to detect faults in a circuit*
- ***CO3****: Determine the testability of a circuit*
- ***CO4:****Design methods/techniques to improve the testability of digital circuits.*
- ***CO5****: Design Logic BIST circuits based on LFSRs*
- ***CO6:*** *Understand various techniques for verification*

Total Hours: 42 Hrs.

Module 1 (10 hours)

Scope of testing and verification in VLSI design process, Issues in test and verification of complex chips, embedded cores and SOCs.

Module 2 (14 hours)
Fundamentals of VLSI testing Fault models. Automatic test pattern generation, Design for testability, Scan design, Test interface and boundary scan. System testing and test for SOCs. Delay fault testing.

Module 3 (9hours)
BIST for testing of logic and memories, Test automation, Design verification techniques based on simulation, analytical and formal approaches.

Module 4 (9hours)
Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking, Hardware emulation.

References:
1. M. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Kluwer Academic Publishers, 2000.
2. M. Abramovici, M. A. Breuer and A. D. Friedman, Digital Systems Testing and Testable Design, IEEE Press, 1990.
3. T.Kropf, Introduction to Formal Hardware Verification, Springer Verlag, 2000.
4.P. Rashinkar, Paterson and L. Singh, System-on-a-Chip Verification-Methodology and Techniques, Kluwer Academic Publishers, 2001.
5. Neil H. E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Second Edition, Addison Wesley, 1993.
6. Neil H. E. Weste and David Harris, Principles of CMOS VLSI Design, Third Edition, Addison Wesley, 2004.

EC6225: Semiconductor Power Devices

Pre-requisites: EC6202

L	T	P/S	C
3	0	0	3

Course Outcomes :

- ***CO1:*** *Understand and model the avalanche break down mechanism in power diodes*
- ***CO2:*** *Describe the applications of power BJT as a switch and explore typical switching applications*
- ***CO3:*** *Understanding operation of Thyristors*
- ***CO4:*** *Studying power MOSFET theory and its applications*

- ***CO5:*** *Simulate power semiconductor devices and understand their I-V and switching characteristics*

Total Hours : 44 Hrs.

Module 1 (10 hours)

Avalanche Breakdown voltage of plane and planar pn junctions, Breakdown voltage improvement Techniques.

High injection level effects in pn junctions. Forward voltage drop in high voltage PIN diodes , and its dependence on carrier lifetime.

Module 2 (14 hours)

Bipolar Power Transistor structures and characteristics, Current-gain, Switching operation, second break down and safe operating area, overlay transistor.

Thyristor operation principles, Reverse and forward blocking voltage and forward conduction characteristics. Cathode shorted and Anode shorted Thyristor. di/dt and dv/dt ratings of thyristors, Triacs and GTO.

Module 3 (14 hours)

Power MOSFET structure, I-V characteristics, on resistance, Minimum size chip design for specific drain breakdown voltage, Switching characteristics, Safe operating area, Insulated Gate Transistor (IGT) – Structure, Operation principle, I-V characteristics and turn off transients, Latch up and its prevention.

Module 4 (6 hours)

Power Integrated Circuit Problems and isolation techniques in HVIC's. Smart PIC's and HVIC's.

References:

1. Baliga, B. Jayant, Power Semiconductor Devices, PWS Publishing Co., Boston, 1996

2. Benda, Vitezslav, John Gowar, and Duncan A. Grant, Chichester , Power semiconductor devices: theory and applications, New York Wiley, c 1999

3. Bose, Bimal K, Modern Power Electronics, Evolution, Technology, and Application, IEEE Press, 1992.

4. Ramshaw, Raymond S., Power Electronics Semiconductor Switches, 2nd ed., London: Chapman & Hall (Kluwer)

5.Rashid, Muhammad H., Upper Saddle River, Power Electronics, Circuits, Devices and Applications, 3rd ed., NJ: Pearson Education, 2003.

EC6226: Nanoelectronics

Pre-requisites: EC6202 or equivalent

L	T	P/S	C
3	0	0	3

Course Outcomes :

- ***CO1****: To explain challenges due to scaling on CMOS devices, VLSI circuit design and fundamental limitsof operation.*
- ***CO2****: To analyze and explain working of novel MOS based silicon devices and various multi gate devices.*
- ***CO3****: To analyze and explain working of SOI devices and their performance comparison with Silicon devices*
- ***CO4****: To understand the underlying concepts by setting up and solving the Schrödinger equation fordifferent types of potentials in one dimension as well as in 2 or 3 dimensions for specific cases.*
- ***CO5****: To understand nanoelectronic systems and building blocks such as: low-dimensional semiconductors, heterostructures, carbon nanotubes, quantum dots, nanowires etc.*
- ***CO6****: Through the mini-project, students should get familiarized with searching for scientific information in their subject area, practice report writing and presenting their project in a seminar*
- ***CO7****: To explain working of spin electronic devices*
- ***CO8****: To summarize the present and future research frontiers of Nanoelectronics and to be able tocritically assess future trends.*

Total Hours: 42 Hrs.

Module 1 (8 hours)

Challenges going to sub-100 nm MOSFETs – Oxide layer thickness, tunneling, power density, non-uniform dopant concentration, threshold voltage scaling, lithography, hot electron effects, sub-threshold current, velocity saturation, interconnect issues, fundamental limits for MOS operation. High-K gate dielectrics, effects of high-K gate dielectrics on MOSFET performance,

Module 2 (12 hours)

Novel MOS-based devices – Multiple gate MOSFETs, Silicon-on-nothing, Silicon-on-insulator devices, FD SOI, PD SOI, FinFETs, vertical MOSFETs, strained Si devices

Module 3 (6 hours)
Hetero structure based devices – Type I, II and III Heterojunction, Si-Ge heterostructure, hetero structures of III-V and II-VI compounds - resonant tunneling devices, MODFET/HEMT

Module 4 (8 hours)
Carbon nanotubes based devices – CNFET, characteristics, Spin-based devices – spinFET, characteristics

Module 5 (8 hours)
Quantum structures – quantum wells, quantum wires and quantum dots, Single electron devices – charge quantization, energy quantization, Coulomb blockade, Coulomb staircase, Bloch oscillations

References:
1. Mircea Dragoman and Daniela Dragoman, Nanoelectronics – Principles & devices, Artech House Publishers, 2005.
2. Karl Goser, Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, Springer 2005.
3. Mark Lundstrom and Jing Guo, Nanoscale Transistors: Device Physics, Modeling and Simulation, Springer, 2005.
4. Vladimir V Mitin, Viatcheslav A Kochelap and Michael A Stroscio, Quantum heterostructures, Cambridge University Press, 1999.
5. S.M. Sze (Ed), High speed semiconductor devices, Wiley, 1990.
6. Manijeh Razeghi, Technology of Quantum Devices, Springer, ISBN 978-1-4419-1055-4.
7. H.R. Huff and D.C. Gilmer, High Dielectric Constant Materials for VLSI MOSFET Applications, Springer 2005, ISBN 978-3-540-21081-8 , (Available on NITC intranet in Springer eBook section)
8.B.R. Nag, Physics of Quantum Well Devices, Springer 2002, ISBN 978-0-7923-6576-1, (Available on NITC intranet in Springer eBook section).
9. E.Kasper, D.J. Paul, Silicon Quantum Integrated Circuits Silicon-Germanium Heterostructures Devices: Basics and Realisations, Springer 2005, ISBN 978-3-540-22050-3, (Available on NITC intranet in Springer eBook section).

EC6227: Low Power VLSI

Pre-requisites: EC6201

L	T	P/S	C
3	0	0	3

Course Outcomes:

- ***CO1****: To explain difference between power and energy.*
- ***CO2****: To identify various leakage sources in a MOSFET and a digital circuit.*
- ***CO3****: To explain various leakage power reduction mechanisms at device level and circuit level.*
- ***CO4****: To calculate various leakage power components in a MOSFET and a digital circuit.*
- ***CO5****: To design a digital circuit by applying leakage power reduction techniques.*
- ***CO6****: To explain various low power design methodologies.*
- ***CO7****: To design a circuit using Sub-Vt design methodology.*
- ***CO8****: To describe, identify and explain adiabatic transitions in a circuit.*

Total Hours: 42 Hrs.

Module 1(12 hours)

Review of power dissipation in CMOS Circuits – static and dynamic power dissipation- Leakage sources, input vector dependence, stack effect, leakage reduction using natural and forced stacks, power gating, power gating methodologies, dynamic voltage scaling, forward and reverse body bias, standby techniques, MTCMOS circuits, level shifters, timing and power planning, choosing the high V_{TH} value, MTCMOS circuits using sleep transistors

Module 2 (14 hours)

Supply voltage scaling approaches: parallelism, pipelining, using multiple supply voltage, module level voltage selection, clustered voltage scaling, level converters, multiple supplies inside a block, supply voltage limitations, Optimum supply voltage, multiple device threshold, Technology level – feature size scaling, threshold voltage scaling, Transistor sizing for energy minimization, dynamic supply voltage scaling, dynamic threshold voltage scaling

Module 3 (6 hours)

Switching activity estimation in static and dynamic logic, signal statistics, intersignal correlations, Reducing switching capacitance through transistor sizing, logic and architecture optimization, layout techniques, logic restructuring, input ordering, data representation, resource allocation, reducing glitching through path balancing, clock gating

Module 4 (10 hours)

Behavioral level transforms, algorithm level transforms, architectural transformations, Operation reduction and substitution, logic level optimization and technology mapping,

Energy recovery, design with reversible logic, adiabatic logic, peripheral circuits, Power gating, signal isolation, state retention and restoration, architectural issues for power gating, Dynamic voltage and frequency scaling.

References:

1. Anantha Chandrakasan, Robert Brodersen, Low-power CMOS design, IEEE press, 1998
2. Kaushik Roy, Sharat C. Prasad, Low-power CMOS VLSI circuit design, John Wiley & Sons, 2000.
3.A.Bellamour, M.I.Elmasri, Low power VLSI CMOS circuit design, Kluwer Academic Press, 1995
4. Siva G.Narendran, Anantha Chandrakasan, Leakage in Nanometer CMOS Technologies, Springer, 2005.
5. Mohab Anis, Mohamed Elmasry, Multi-Threshold CMOS Digital Circuits, Kluwer Academic Publishers, 2003.
6. Michael Keating, David Flynn, Robert Aitken, Alan Gibbons and Kaijian Shi, Low power methodology manual, Springer, 2008.

EC6228: Mixed Signal Circuit Design

Pre-requisites: EC6204

L	T	P/S	C
3	0	0	3

Course Outcomes:

- ***CO1:****Understanding the non-idealities and quantitative design metrics of data converters*
- ***CO2:*** *Understanding the working and designing of continuous and discrete time building blocks used in the design of data converters*
- ***CO3:****Analyzing the data converter architectures and choosing the suitable data converter for the given application*
- ***CO4:*** *Achieving system level specifications with transistor level design using CAD tools*
- ***CO5:*** *Studying different types of PLLs*

Total Hours: 42 Hrs.

Module 1 (9 hours)
CMOS comparators-Introduction to switched capacitor circuits - basic building blocks – operation and analysis – non ideal effects in switched capacitor circuits-switched capacitor integrators - First order filters – switch sharing – biquad filters.

Module 2 (10 hours)
Basic PLL topology, dynamics of simple PLL, Multiplier, EXOR and JK –flipflop phase detectors, lock acquisition, Phase frequency detector, Loop filters, Charge Pump PLLs, non ideal effects in PLLs.

Module 3 (13 hours)
Data converter fundamentals – DC and dynamic specifications – quantization noise – Nyquist rate D/A converters – decoder based converters – binary scaled converters – thermometer code converters – hybrid converters- Nyquist rate A/D converters-Successive approximation, Flash, interpolating, Folding, Pipelined, Time-interleaved converters

Module 4 (10 hours)
Oversampling converters, Noise shaping modulators, Decimating filters and interpolating filters, Higher **order** modulators, Delta Sigma modulators with multibit quantizers- Delta Sigma D/A

References:
1. Behzad Razavi, Design of Analog CMOS Integrated Circuit, Tata-Mc GrawHill, 2002.
2. Rudy van de Plassche, CMOS integrated Analog- to Digital and Digital to- Analog converters, Kluwer academic publishers,2003.
3. David Johns, Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons, 2001.
4. Roland E.Best, Phase Locked Loops, McGraw Hill,2007.
5. Richard Schreier, Understanding Delta-Sigma Data Converters, Wiley Interscience, 2005.
6. R.Jacob Baker, CMOS Mixed-signal Circuit Design, Wiley Student Edition, Wiley Interscience, 2009.

EC6229: Selected Topics In Circuit Design

Pre-requisites: EC6204

L	T	P/S	C
3	0	0	3

EC6230: CMOS RF Circuit Design

Pre-requisites: EC6204

L	T	P/S	C
3	0	0	3

Course Outcomes:

- ***CO1:*** *Understanding passive components at RF frequencies and required circuit theory for analysis*
- ***CO2:*** *Studying high frequency amplifier design techniques and low noise amplifier configurations*
- ***CO3:*** *Designing low power and high linearity RF amplifiers using CAD tools*
- ***CO4:*** *Understanding the design considerations of frequency synthesizers at RF frequencies*
- ***CO5:*** *Identifying the sources of phase noise and understanding phase noise reduction techniques*

Total Hours: 42 Hrs.

Module 1 (12 hours)

Characteristics of passive IC components at RF frequencies – interconnects, resistors, capacitors, inductors and transformers – Transmission lines Classical two-port noise theory, noise models for active and passive components, Noise figure, Friis equation, Nonlinearity and cascaded stages, Sensitivity and dynamic range, Passive impedance transformation.

Module 2 (12 hours)

High frequency amplifier design – zeros as bandwidth enhancers, shunt-series amplifier, fT doublers, neutralization and unilateralization Low noise amplifier design – LNA topologies, impedance matching, power constrained noise optimization, linearity and large signal performance, noise canceling LNAs, Constant gm biasing, current reusing technique.

Module 3 (10 hours)

Mixers – multiplier-based mixers, subsampling mixers, diode-ring mixers

RF power amplifiers – Class A, AB, B, C, D, E and F amplifiers, modulation of power amplifiers, linearity considerations.

Module 4 (8 hours)

Oscillators & synthesizers – describing functions, resonators, negative resistance oscillators, synthesis with static moduli, synthesis with dithering moduli, combination synthesizers – phase noise considerations.

References:

1. Thomas H. Lee, Cambridge, The Design of CMOS Radio-Frequency Integrated Circuits, UK: Cambridge University Press, 2004.
2. Behzad Razavi, RF Microelectronics, Prentice Hall, 1998.
3. A.A. Abidi, P.R. Gray, and R.G. Meyer, eds. Integrated Circuits for Wireless Communications, New York: IEEE Press, 1999.
4. Bosco Leung and Charles G. Sodini, VLSI for wireless communication, Second Impression, Pearson, 2009.